

1/19

100

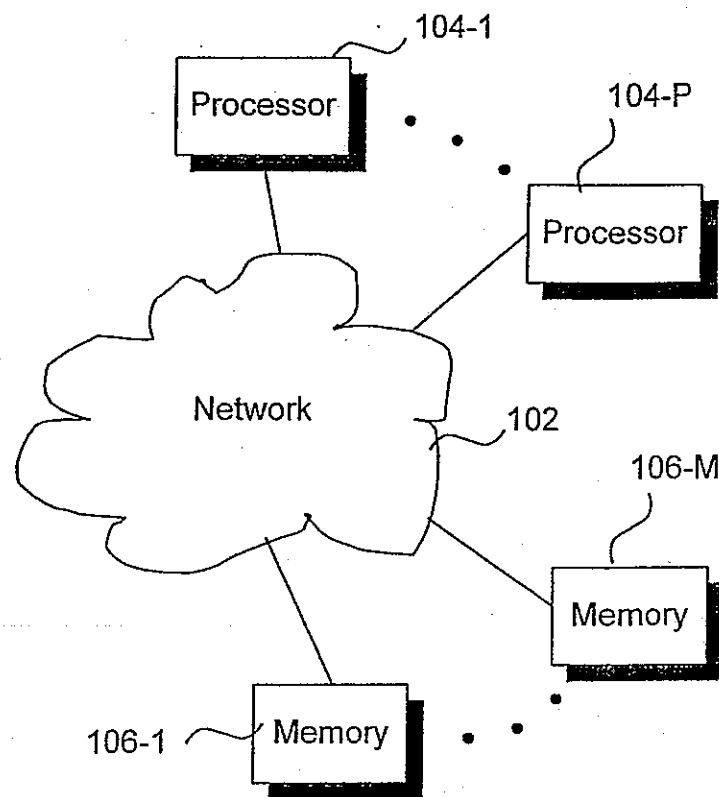


FIG. 1

2/19

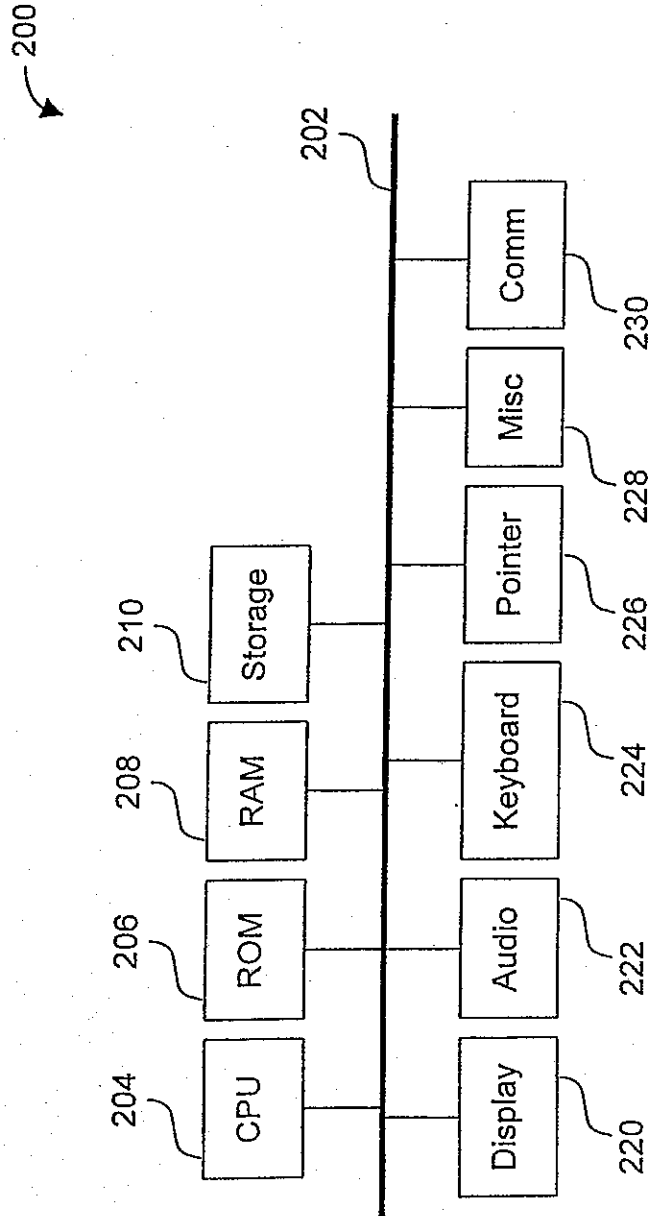


FIG. 2

3/19

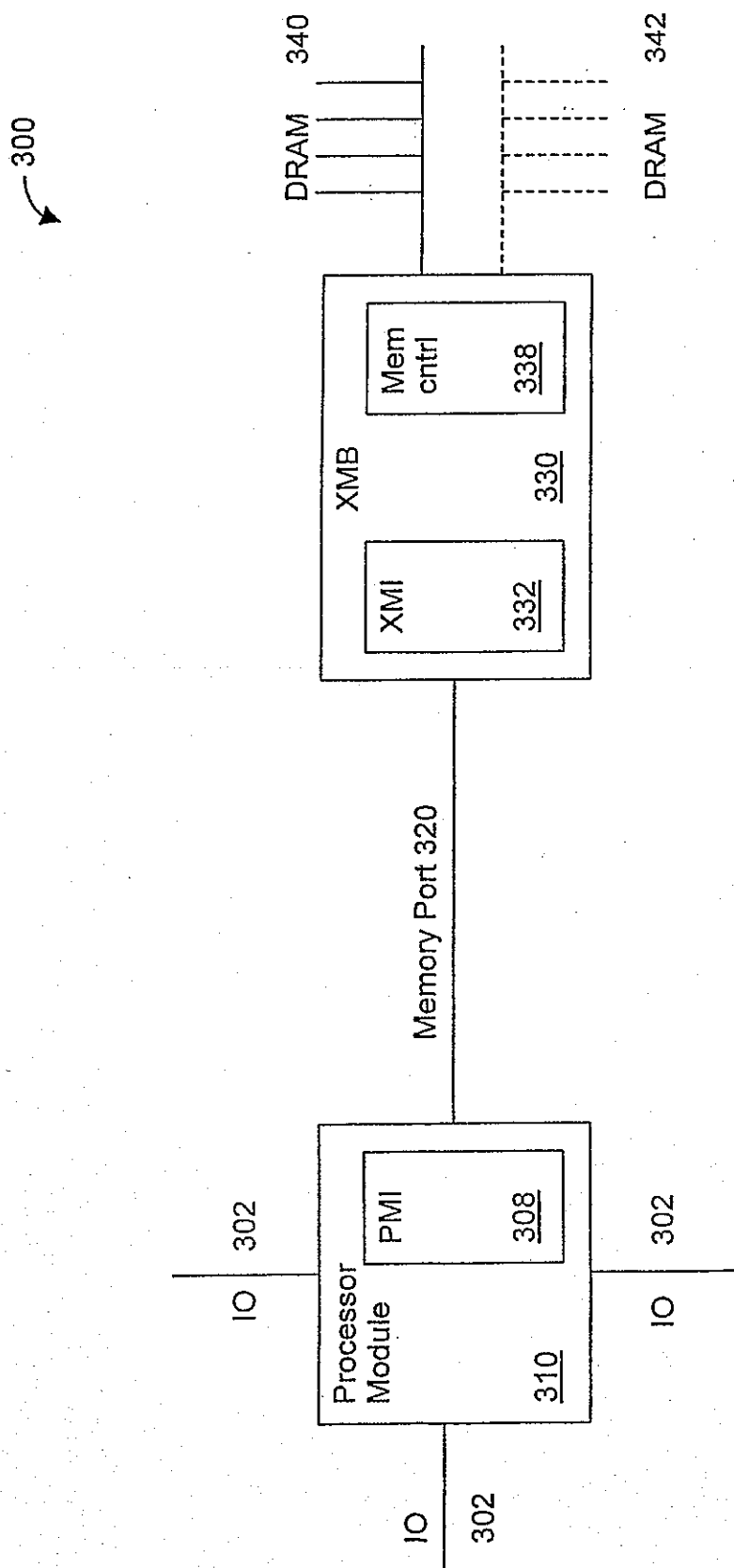


FIG. 3

4/19

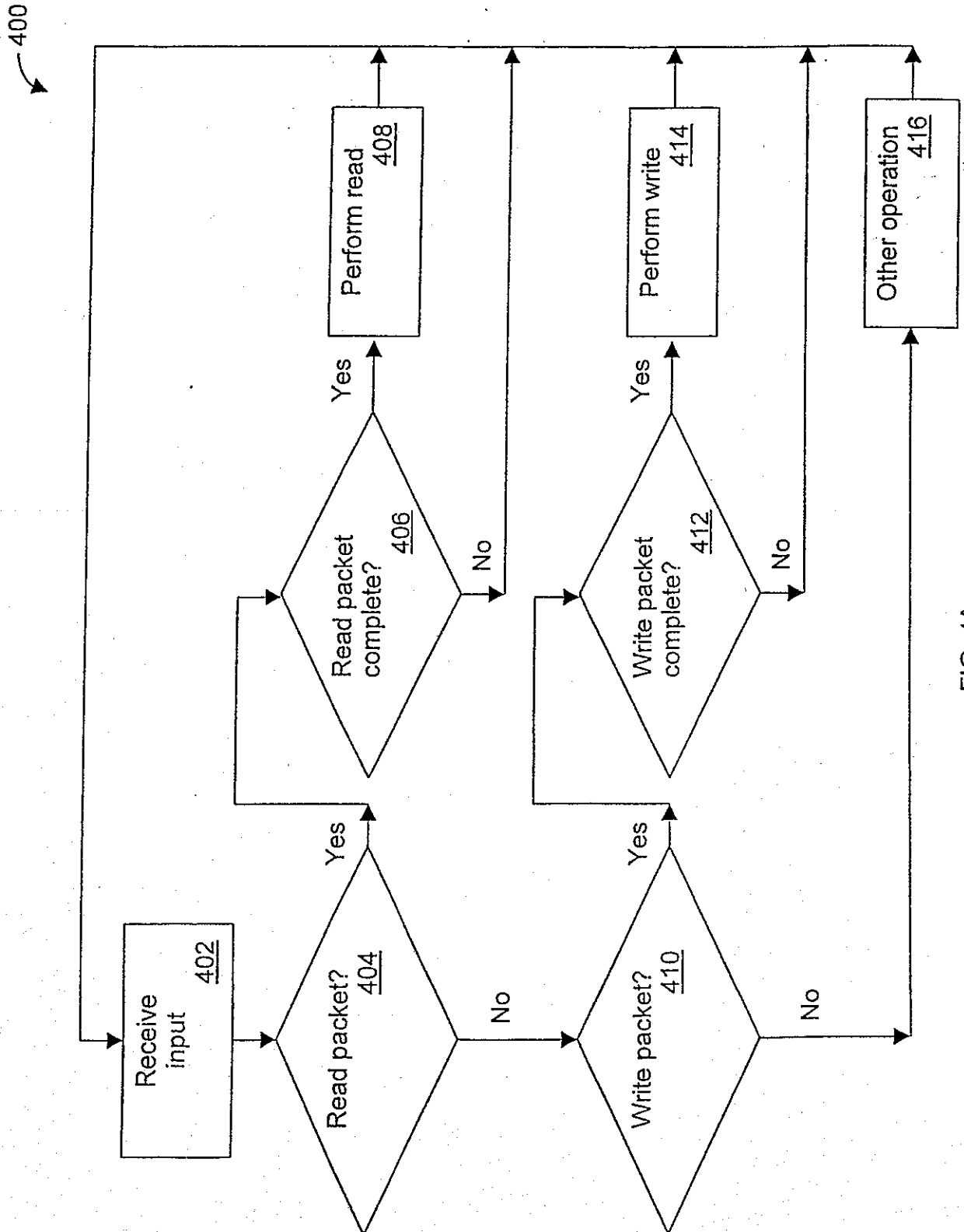


FIG. 4A

5/19

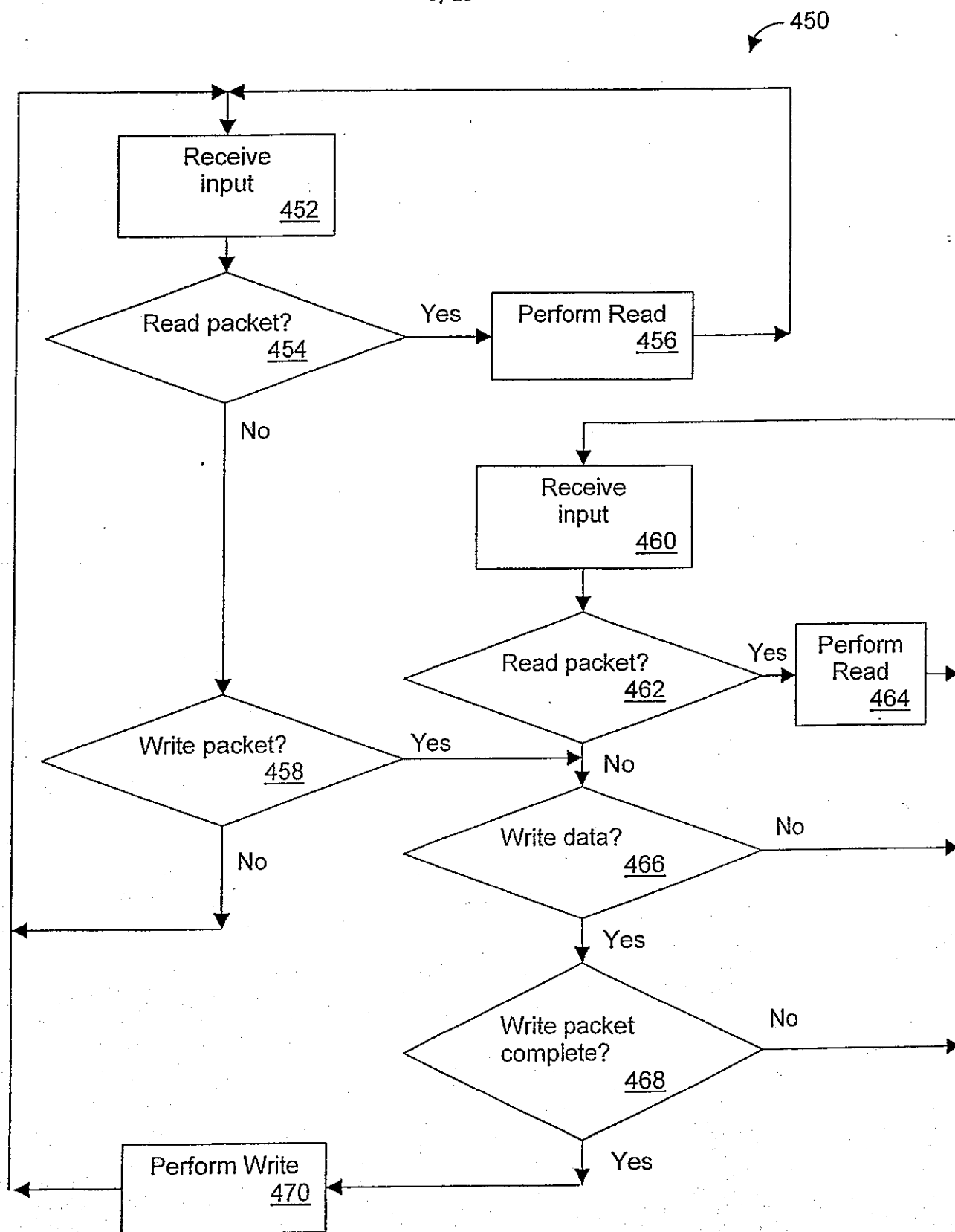
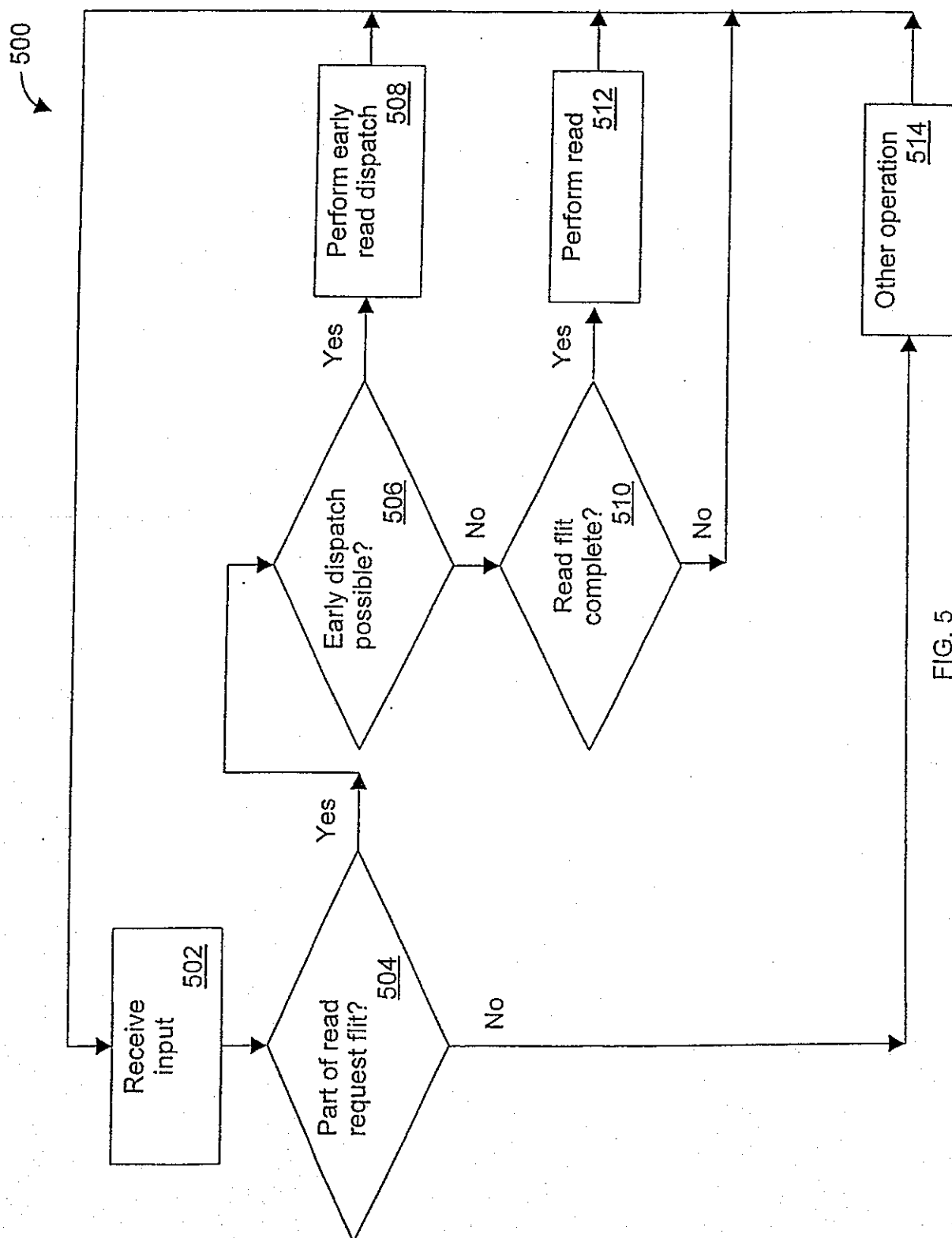


FIG. 4B

6/19



7/19

600

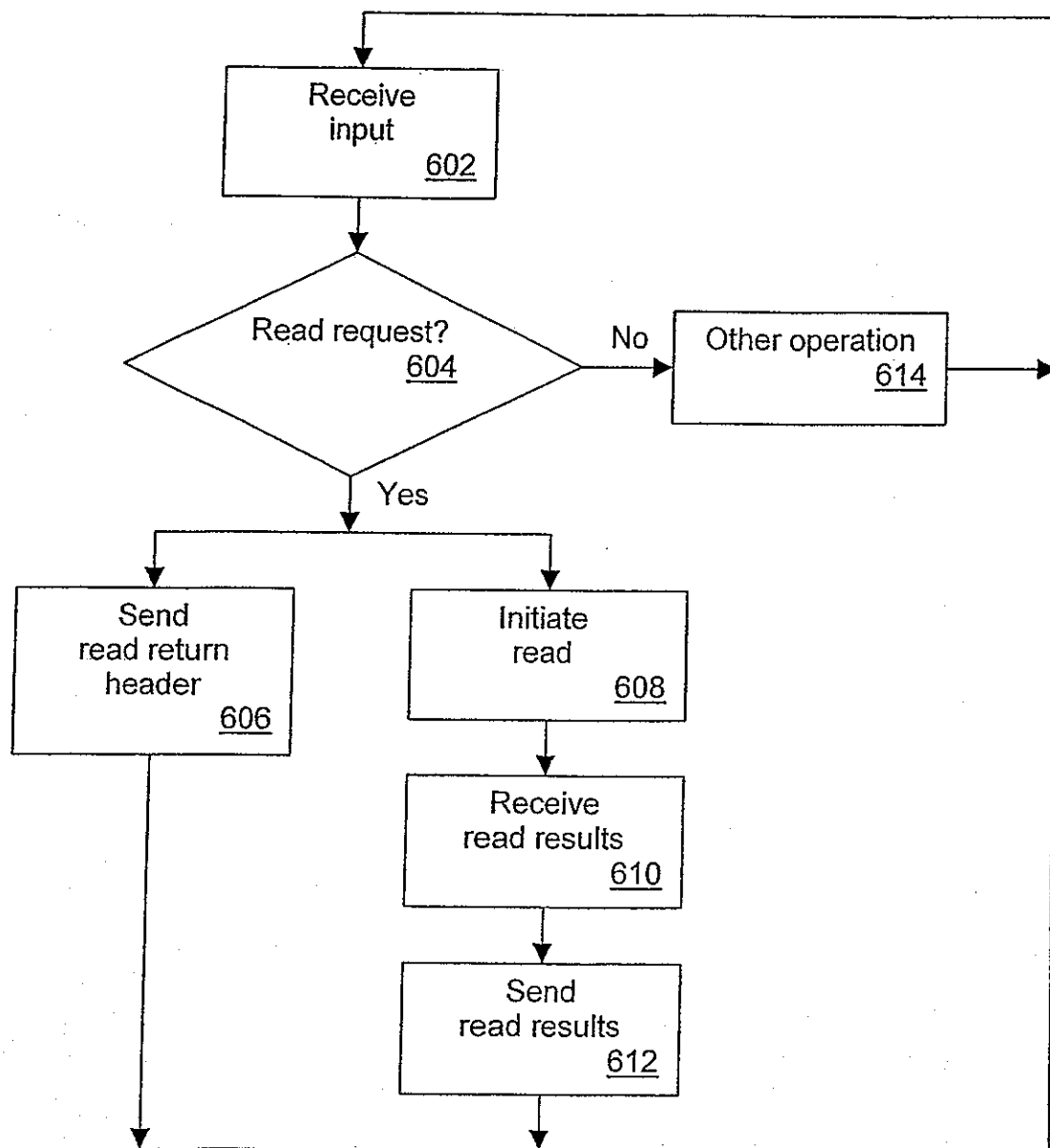


FIG. 6A

8/19

650

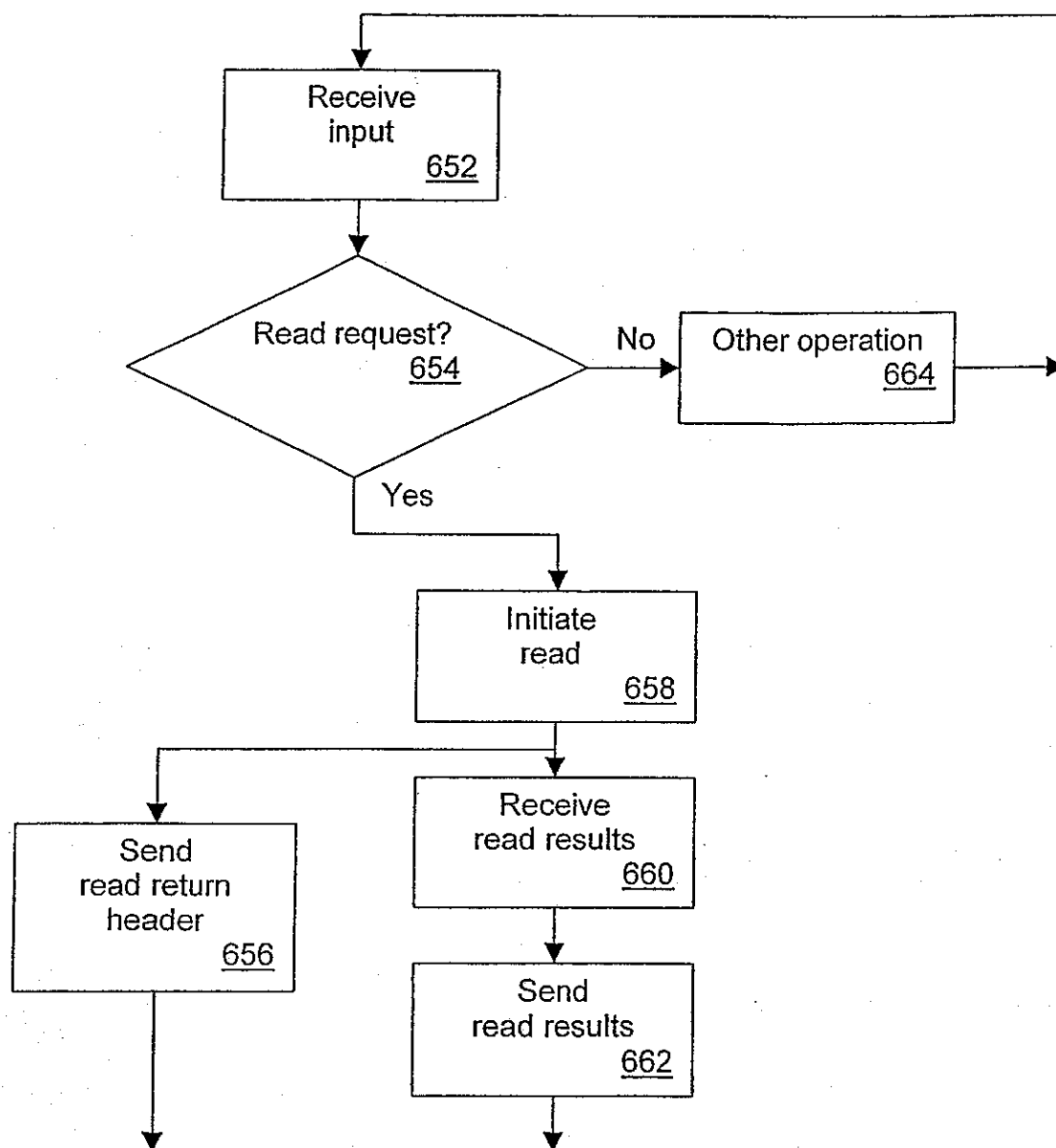


FIG. 6B

9/19

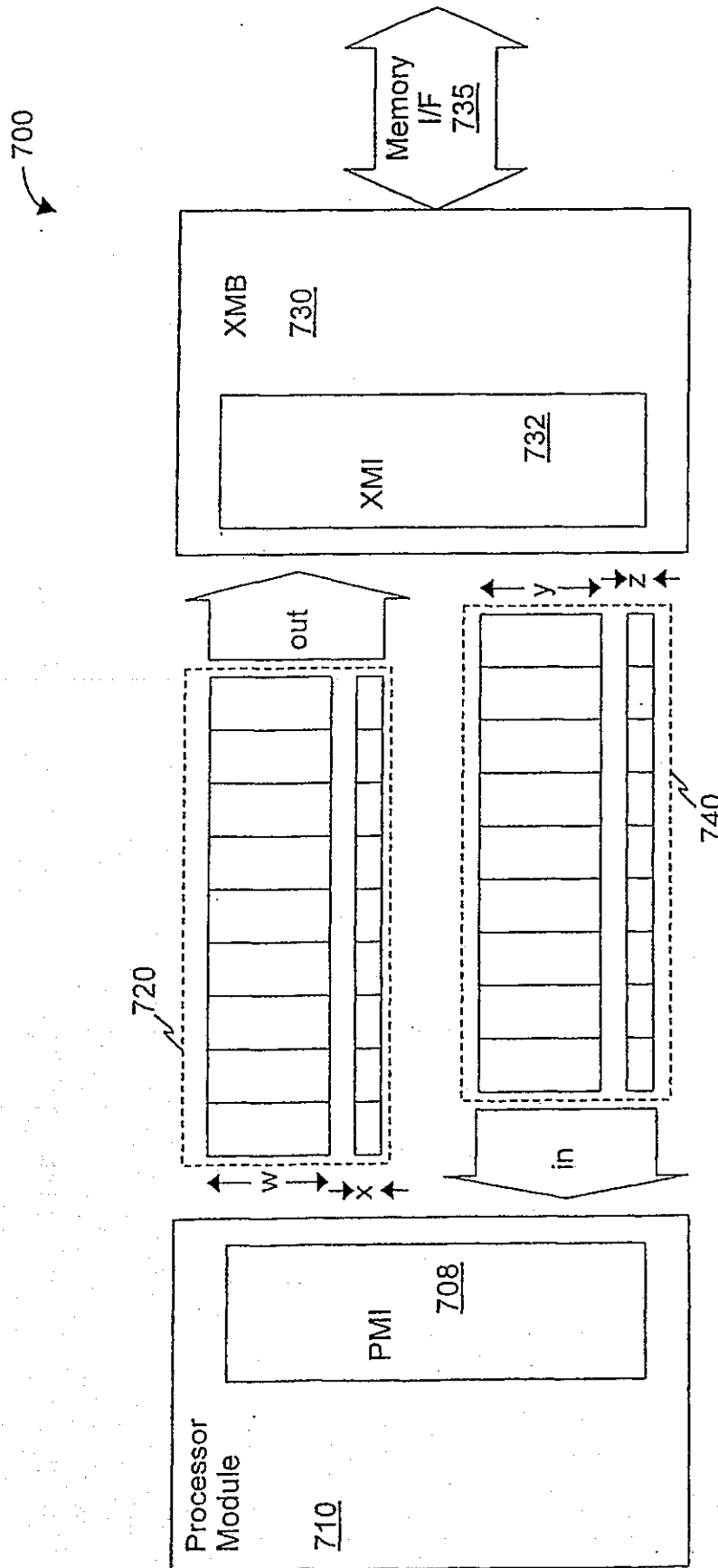


FIG. 7

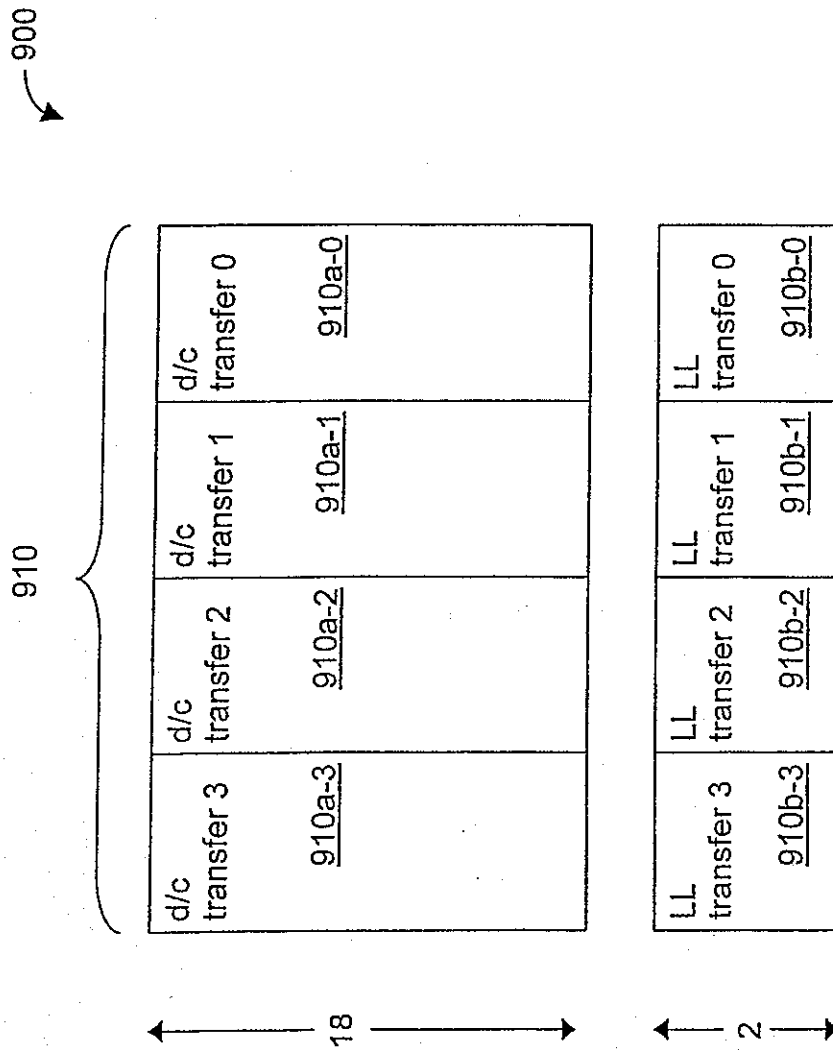


FIG. 9

12/19

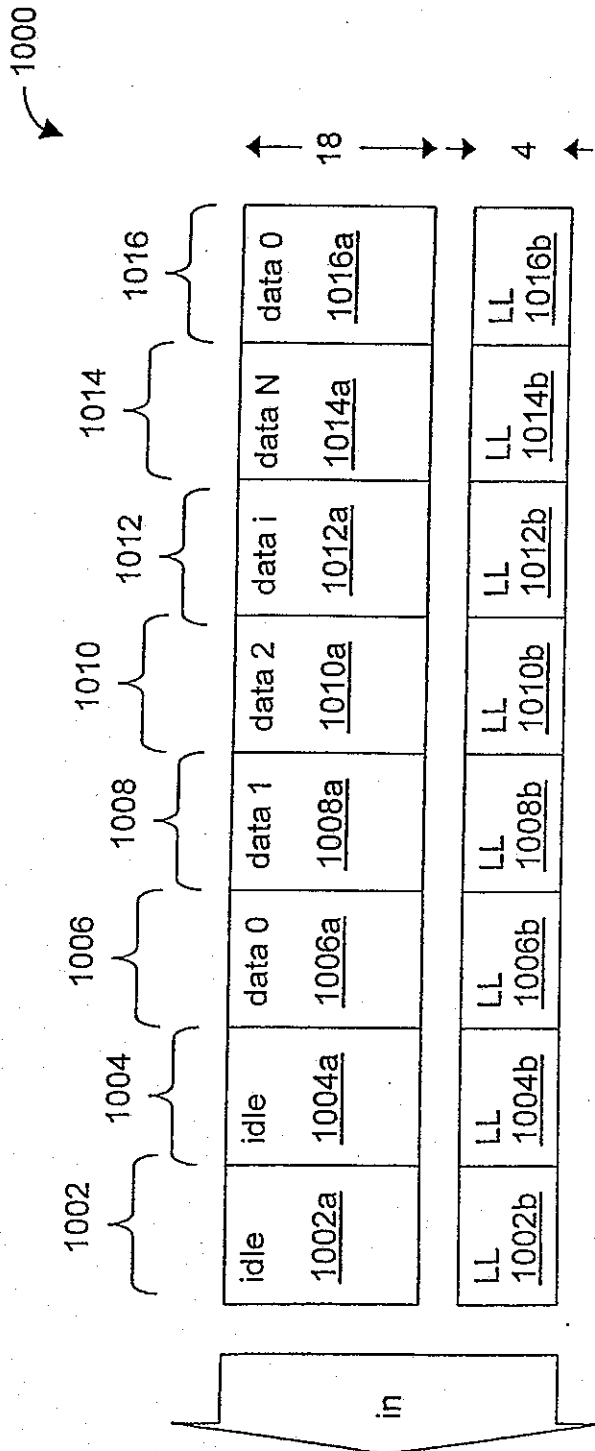


FIG. 10

13/19

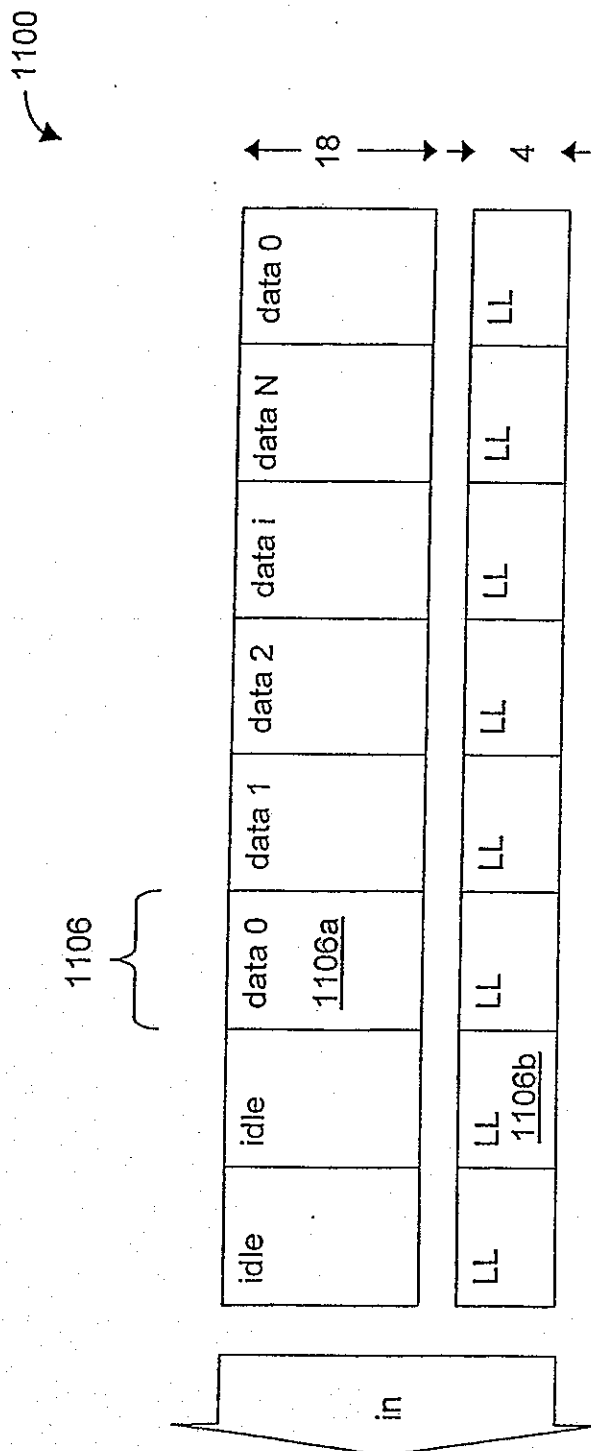


FIG. 11

14/19

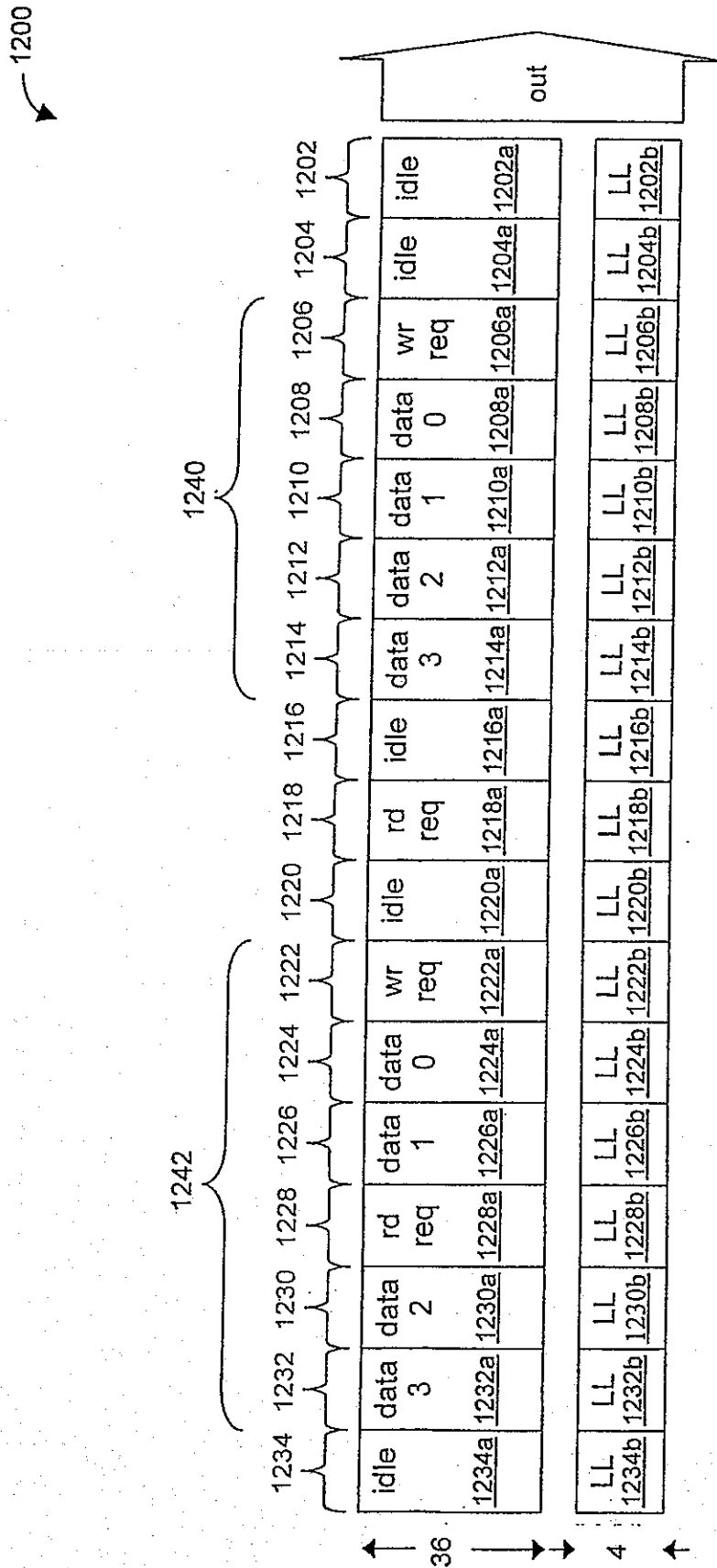


FIG. 12

15/19

1300

↓Transfer	BITS 17:0
0	Lower Order Address Bits and Read/Write Command
1	Higher Order Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Stream ID,
3	Size Bits, Cancel Command, Priority, etc.

FIG. 13

1400

↓ Transfer	BITS 17:0
0	Lower Order Address Bits and Read/Write Command
1	Higher Order Address Bits and Early Read Indicator
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, Size Bits, etc.
3	

FIG. 14

17/19

1500

↓Transfer	BITS 17:0	
0	Lower Order Configuration Address Bits and Read/Write Command	
1	Higher Order Configuration Address Bits and Early Read Indicator	
2	Command Destination, Offset from Address, Transaction ID, Check Bits, Mask Bits, etc.	
3		

FIG. 15

18/19

1600

LL signals	Transfers 0:3
0	Info and Check Bits
1	Header, Tail, and Check Bits
2	Extended Mode Bits
3	

FIG. 16

1700

LL signals	Transfers 0:3
0	Type and Check Bits
1	
2	Info and Check Bits
3	

FIG. 17

1800

LL signals	Transfers 0:3
0	Tag, Control, and Check Bits
1	
2	Tag, Info, and Check Bits
3	

FIG. 18

1900

LL signals	Transfers 0:3
0	Tag and Check Bits
1	
2	Tag, Info, and Check Bits
3	

FIG. 19

2000

LL signals	Transfers 0:3
0	Signal and Check Bits
1	
2	Signal, Info, Stop, and Check Bits
3	

FIG. 20