

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
24 July 2025 (24.07.2025)



(10) International Publication Number
WO 2025/151958 A1

(51) International Patent Classification:
G06N 10/40 (2022.01) *H10N 60/81* (2023.01)
H10D 62/00 (2025.01)

(21) International Application Number:
PCT/CA2025/050062

(22) International Filing Date:
16 January 2025 (16.01.2025)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/621,143 16 January 2024 (16.01.2024) US

(71) Applicant: ANYON SYSTEMS INC. [CA/CA]; 1985
55th Avenue, Suite 100, Dorval, Québec H9P 1G9 (CA).

(72) Inventor: NAJAFI-YAZDI, Alireza; 139 rue Bach, Vau-
dreuil-Dorion, Québec J7V 0M7 (CA).

(74) Agent: NORTON ROSE FULBRIGHT CANADA
S.E.N.C.R.L., S.R.L. / LLP; 2500-1 Place Ville-Marie,
Montréal, Québec H3B 1R1 (CA).

(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG,
KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY,
MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA,
NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO,
RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,

(54) Title: THREE-DIMENSIONAL ARCHITECTURES FOR LARGE-SCALE QUANTUM PROCESORS

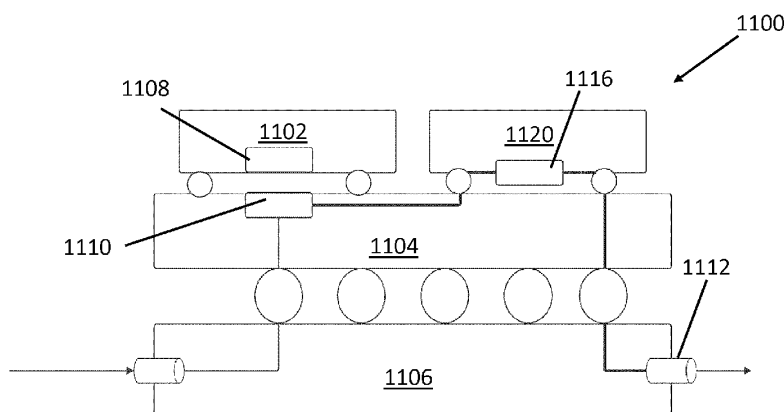


FIG. 11

(57) Abstract: There is described herein a superconducting quantum processor package comprising: a package substrate having an external connector port; an interposer having first and second opposing surfaces, the first surface of the interposer facing the package substrate, the interposer carrying a first quantum readout device coupled to the external connector port; a first qubit substrate having top and bottom opposing surfaces, the bottom surface of the first qubit substrate facing the second surface of the interposer, the first qubit substrate carrying a first qubit circuit with interleaved qubits and couplers, the first qubit circuit coupled to the first quantum readout device, wherein the first qubit circuit, the first quantum readout device, and the external connector port form a first readout communication path; and a first amplifying device in the first readout communication path, coupled between the first quantum readout device and the external connector port, to amplify readout signals from the first quantum readout device.

[Continued on next page]

WO 2025/151958 A1

TJ, TM, TN, TR, TT, TZ, UA, UG, US, UY, UZ, VC, VN,
WS, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- *with international search report (Art. 21(3))*
 - *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*
 - *in black and white; the international application as filed contained color or greyscale and is available for download from PATENTSCOPE*
-