

CLAIMS

We claim:

1. A glass wafer for a semiconductor device (100), comprising:
a glass substrate comprising: a top surface (102), a bottom surface (104) opposing the top surface, and an edge surface (106) between the top surface and the bottom surface;
a first coating (108) disposed atop the glass substrate, wherein the first coating is a doped crystalline silicon coating having a sheet-resistance of 100 to 1,000,000 ohm per square; and
a second coating (110) having one or more layers disposed atop the glass substrate, wherein the second coating comprises a silicon containing coating,
wherein the glass wafer has an average transmittance (T) of less than 50% over an entire wavelength range of 400 nm to 1000 nm.
2. The glass wafer of claim 1, wherein a transmittance at every wavelength in the wavelength range is less than 50%.
3. The glass wafer of claim 1, wherein the glass wafer has an average transmittance (T) of less than 50% over an entire wavelength range of 400 nm to 2500 nm.
4. The glass wafer of claim 3, wherein a transmittance at every wavelength in the wavelength range is less than 50%.
5. The glass wafer of claim 1, wherein the glass wafer has a transmittance (T) of less than 30% over an entire wavelength range of 400 nm to 1000 nm.
6. The glass wafer of claim 5, wherein a transmittance at every wavelength in the wavelength range is less than 30%.
7. The glass wafer of claim 1, wherein the glass wafer has a transmittance (T) of less than 30% over an entire wavelength range of 400 nm to 2500 nm.

8. The glass wafer of claim 7, wherein a transmittance at every wavelength in the wavelength range is less than 30%.
9. The glass wafer of claim 1, wherein the first coating is disposed directly atop the top surface of the glass substrate and the second coating is disposed directly atop the first coating.
10. The glass wafer of claim 1, wherein the second coating comprises at least two layers and wherein the first coating is located between the at least two layers of the second coating.
11. The glass wafer of claim 1, wherein the doped crystalline silicon coating is one of a phosphorus-doped crystalline silicon, a boron-doped crystalline silicon, or an arsenic doped-crystalline silicon.
12. The glass wafer of claim 1, wherein a total thickness of the doped crystalline silicon coating and the second coating is less than 1000 micron (10000 angstrom).
13. The glass wafer of claim 12, wherein the doped crystalline silicon coating has a thickness of at least 100 angstrom.
14. The glass wafer of claim 1, wherein the second coating comprises: a layer of undoped amorphous silicon.
15. The glass wafer of claim 1, wherein the second coating comprises: a layer of silicon nitride, a layer of undoped amorphous silicon, and a layer of silicon dioxide,
wherein the layer of silicon nitride is disposed atop the layer of undoped amorphous silicon,
wherein the layer of undoped amorphous silicon is disposed atop the layer of silicon dioxide, and
wherein the layer of silicon dioxide is atop the doped crystalline silicon coating.
16. The glass wafer of claim 1, further comprising a passivation coating (112) atop the top surface, bottom surface, and edge surface of the glass substrate.

17. The glass wafer of claim 16, wherein the passivation coating is one of SiN, SiO₂, or SiON.
18. The glass wafer of claim 17, wherein the passivation coating has a thickness of 100 to 10,000 angstroms.
19. A glass wafer (100) for a semiconductor device, comprising:
 - a glass substrate comprising: a top surface (102), a bottom surface (104) opposing the top surface, and an edge surface (106) between the top surface and the bottom surface; and
 - a coating (110) having one or more layers disposed atop the glass wafer, wherein the coating comprises a silicon containing coating, and wherein the glass wafer has an average transmittance (T) of less than 50% over an entire wavelength range of 400 nm to 1000 nm.
20. The glass wafer of claim 19, wherein the coating covers an entire top surface of the glass substrate.
21. The glass wafer of claim 19, wherein the coating covers a portion of the top surface of the glass substrate from the edge surface to a radial distance 2 mm toward a center of the top surface.
22. The glass wafer of claim 19, wherein a transmittance at every wavelength in the wavelength range is less than 50%.
23. The glass wafer of claim 19, wherein the glass substrate has an average transmittance (T) of less than 50% over an entire wavelength range of 400 nm to 2500 nm.
24. The glass wafer of claim 23, wherein a transmittance at every wavelength in the wavelength range is less than 50%.
25. The glass wafer of claim 19, wherein the glass wafer has an average transmittance (T) of less than 30% over an entire wavelength range of 400 nm to 2500nm.
26. The glass wafer of claim 25, wherein a transmittance at every wavelength in the wavelength range is less than 30%.

27. The glass wafer of claim 19, wherein the glass wafer has an average transmittance (T) of less than 30% over an entire wavelength range of 400 nm to 1000nm.
28. The glass wafer of claim 27, wherein a transmittance at every wavelength in the wavelength range is less than 30%.
29. The glass wafer of claim 19, wherein a thickness of the coating is less than 1 micron.
30. The glass wafer of claim 19, wherein the coating comprises: a layer of undoped amorphous silicon.
31. The glass wafer of claim 19, wherein the coating comprises: a layer of silicon nitride, a layer of undoped amorphous silicon, and a layer of silicon dioxide,
wherein the layer of silicon nitride is disposed atop the layer of undoped amorphous silicon,
wherein the layer of undoped amorphous silicon is disposed atop the layer of silicon dioxide.
32. The glass wafer of claim 19, further comprising a passivation coating (112) atop the top surface, bottom surface, and edge surface of the glass substrate.
33. The glass wafer of claim 32, wherein the passivation coating is one of SiN, SiO₂, or SiON.
34. The glass wafer of claim 32, wherein the passivation coating has a thickness of 100 to 10,000 angstroms.
35. A method of fabricating an electronic device, the method comprising:
loading a glass wafer onto a substrate support within a substrate aligner chamber,
wherein the substrate aligner comprises a light source, and an optical sensor configured to detect a light beam from the light source,
wherein the glass wafer comprises: a glass substrate comprising: a top surface (102), a bottom surface (104) opposing the top surface, and an edge surface (106)

between the top surface and the bottom surface, a first coating (108) disposed atop the glass substrate, wherein the first coating is a doped crystalline silicon coating having a sheet-resistance of 100 to 1,000,000 ohm per square, and a second coating (110) having one or more layers disposed atop the glass substrate, wherein the second coating comprises a silicon containing coating, wherein the glass wafer has an average transmittance (T) of less than 50% over an entire wavelength range of 400 nm to 1000 nm;

rotating the substrate support to position the glass wafer in a predetermined position in the substrate aligner chamber, wherein the predetermined position is reached when the optical sensor detects the light beam from the light source; and

transferring the glass wafer to a semiconductor processing chamber for further processing.

36. A glass wafer for a semiconductor device, comprising:

a glass substrate comprising: a top surface (102), a bottom surface (104) opposing the top surface, and an edge surface (106) between the top surface and the bottom surface; and

a silicon containing coating disposed on the glass substrate, wherein the silicon containing coating comprises at least two silicon containing layers, and wherein a difference in the refractive index values of adjacent layers is greater than 0.5.

37. The glass wafer of claim 36, wherein the coating comprises: a layer of silicon nitride, a layer of undoped amorphous silicon, a layer of silicon dioxide, and a phosphorus-doped crystalline silicon layer, wherein the layer of silicon nitride is disposed atop the layer of undoped amorphous silicon, wherein the layer of undoped amorphous silicon is disposed atop the layer of silicon dioxide, wherein the layer of silicon dioxide is disposed atop the phosphorus-doped crystalline silicon layer.