ABSTRACT

SELF-ALIGNED ELEVATED TRANSISTOR

A method of forming a a self-aligned elevated transistor using selective epitaxial growth is described. An oxide layer is provided overlying a semiconductor substrate. The oxide layer is etched through to the semiconductor substrate to form a trench having a lower portion contacting the substrate and an upper portion having a width larger than the width of the lower portion. A silicon layer is grown within the trench using selective epitaxial growth wherein the silicon layer fills the lower portion and partially fills the upper portion. Nitride spacers are formed on the sidewalls of the trench. A polysilicon layer is deposited overlying the oxide layer and within the trench and etched back to form a gate electrode within the trench between the nitride spacers. The nitride spacers are etched away where they are not covered by the gate electrode leaving thin nitride spacers on sidewalls of the gate electrode. Ions are implanted into the silicon layer exposed at the edges of the trench whereby source and drain pockets are formed within the silicon layer wherein the junction depth is determined by the thickness of the silicon layer. A dielectric layer is deposited overlying the oxide layer and the gate electrode and source/drain pockets within the trench to complete formation of the self-aligned elevated transistor in the fabrication of an integrated circuit.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)