

ABSTRACT

A semiconductor device includes a memory cell structure in a cell array region, an electrode stacking structure including a plurality of electrodes and a plurality of interlayer insulation layers alternately stacked in a connection region, and a plurality of electrode contact portions penetrating at least a partial portion of the electrode stacking structure and are electrically connected to the plurality of electrodes. The plurality of electrode contact portions include first and second contact portions. The first contact portion includes a first conductive portion, and a first side insulation layer between the electrode stacking structure and the first conductive portion. The second contact portion includes a second conductive portion, and a second side insulation layer between the electrode stacking structure and the second conductive portion. The second side insulation layer has a shape or a structure different from a shape or a structure of the first side insulation layer.

FIG. 1