# "METHOD FOR RECOVERING THE DIGITAL ERROR OF A DIGITAL ARRAY ANTENNA AFTER POWERING IT OFF/ON AGAIN"

## Cross-Reference to Related Applications

This Patent Application claims priority from European Patent Application No. 21425030.0 filed on June 17, 2021 and from Italian Patent Application No. 102022000010826 filed on May 24, 2022, the entire disclosure of which is incorporated herein by reference.

## Technical field of the invention

The present invention relates to a method for recovering the digital error of a digital array antenna after powering it off/on again and a corresponding digital array antenna. In particular, the present invention finds advantageous, but not exclusive application in a full digital array radar, (Full DAR), to which the following description will make explicit reference without thereby losing generality.

## State of the art

As is well known, a digital array antenna of a Full DAR comprises a plurality of radiating elements arranged in an array, a plurality of transmitting/receiving modules, which are adapted to operate at a plurality of radio frequencies and each of which is connected to a respective radiating element, a signal generation and conversion module for generating baseband signals and converting to and from radio frequency, a processor, which is adapted to control the signal generation and conversion module, a clock generator, which provides a reference clock to the processor (5), to the signal generation and conversion module and to the transmitting/receiving modules.

The signal generation and conversion module comprises a baseband or intermediate band section and a conversion section for converting signals to and from radio frequency. Each transmitting/receiving module comprises a transmitting branch and a receiving branch both of which are connected between the relative radiating element and the signal generation and conversion module.

In particular, the signal generation and conversion module is of the digital type, e.g. comprising a suitably configured FPGA module, the transmitting branch of the transmitting/receiving module comprises a digital-to-analogue converter (DAC) interfaced with the signal generation and conversion module and a high-power amplifier (HPA) connected between the digital-to-analogue converter and the radiating element, and the receiving branch comprises a low-noise amplifier (LNA) connected with the radiating element and an analogue-to-digital converter (ADC) connected between the

low-noise amplifier and the signal generation and conversion module. The DAC and ADC converters of the transmitting/receiving modules, as well as the signal generation and conversion module, sample the reference clock in order to maintain synchronism between them and the processor.

Before it can be used, a digital array antenna must be calibrated in order to generate an equiphase plane on the antenna regardless of the radio frequency transmitted by the antenna to produce a certain radiation pattern and enable pointing thereof. Calibration serves to compensate for all electromagnetic and digital differences between the different transmitting/receiving modules and the radiating elements, e.g. slight physical imperfections of the different radiating elements, as well as different delays due to different signal feed paths between the signal generation and conversion module and the radiating elements. Calibration basically consists of determining the signal phases to be applied to the radiating elements for each of the radio frequencies used by the digital array antenna. The determined phases are set on the signal generation and conversion module. Calibration has a high execution time as the frequencies of a Full DAR to be measured can be of the order of one hundred.

When the digital array antenna is powered off and on again, all the transmitting/receiving modules sample the reference clock again, and it is highly probable that some transmitting/receiving module delays or anticipates the sampling, thus producing a time translation of some clock period for some antenna elements that causes the equiphase plane condition to be lost. In other words, clock metastability produces digital errors that corrupt antenna performance. Therefore, after each powering off/on again, the digital array antenna must be calibrated at all radio frequencies again before becoming operational again, resulting in a considerable loss of time. This is highly undesirable for a Full DAR that often finds itself operating in critical environments where maximum efficiency is required.

Chinese patent application No. CN112731315A discloses a rapid amplitude-phase calibration system and method for large-array-plane digital array radar. The system comprises a control module, a calibration module, an internal calibration network, a digital TR assembly and an optical communication network. The control module communicates with the calibration module and the digital TR assembly through optical fibers and is used for calibration control, signal coding and calibration data acquisition. The calibration module is used for opening a receiving channel, receiving a calibration signal transmitted by the array plane TR assembly, generating a sampling trigger to carry out data sampling and reporting sampling data to the control module according to a

protocol when the system carries out transmission calibration. When the system carries out receiving calibration, a transmitting calibration signal is generated and output according to a code and a control signal transmitted by the control module. The internal calibration network comprises a radio frequency cable network and a power divider, and is used for connecting the radio frequency channel of the calibration module with the radio frequency channel of each digital TR assembly on the array plane for internal calibration test of the system. When the number of array plane channels is relatively large, the power-on preparation time of equipment can be remarkably reduced.

## Subject and Summary of the Invention

Aim of the present invention is to provide a method that allows quickly recalibrating a digital array antenna and which, at the same time, is easy and inexpensive to implement.

In accordance with the present invention there are provided a method for recovering the digital error of a digital array antenna, in particular for a digital array radar, after powering off/on again and a digital array antenna, in particular for a digital array radar, as defined in the appended claims.

## Brief description of the Drawings

Figure 1 shows a simplified block diagram of a digital array antenna implementing the method of the present invention for recovering the digital error of a digital array antenna after powering it off/on again.

Figure 2 shows a block diagram of a transmitting/receiving module of the digital array antenna of Figure 1 during a particular operating phase of the method of the invention.

Figure 3 is a concise flow chart showing the main phases of the method of the present invention

## Detailed Description of Preferred Embodiments of the Invention

In Figure 1, 1 generically denotes as a whole a digital array antenna, in particular for a digital radar, e.g. a full DAR. The antenna 1 comprises a plurality of radiating elements 2, a corresponding plurality of transmitting/receiving modules 3, which are adapted to operate at a plurality of radio frequencies and each of which is connected to a respective radiating element 2, a signal generation and conversion module 4 for generating baseband or intermediate band signals and converting to and from radio frequency, a processor 5, which comprises a non-volatile memory 6 and is adapted to control the signal generation and conversion module 4, and a clock generator 7, which provides a reference clock to the processor 5, to the signal generation and conversion module 4 and to the transmitting/receiving modules 3.

For the sake of ease of description, Nf will hereafter denote the number of the aforesaid radio frequencies and Nk will denote the number of radiating elements. The number of radio frequencies Nf is in the order of a hundred.

The signal generation and conversion module 4 comprises a base or intermediate band section 8 and a conversion section 9 for converting signals to and from radio frequency. Each transmitting/receiving module 3 comprises a transmitting branch 10 and a receiving branch 11 both of which are connected between the relative radiating element 2 and the signal generation and conversion module 4.

In particular, the signal generation and conversion module 4 is of the digital type, for example it comprises a suitably configured FPGA module. The transmitting branch 10 of each transmitting/receiving module 3 comprises, connected in cascade towards the relative radiating element 2, a digital-to-analogue converter (DAC) 12 and a high-power amplifier (HPA) 13. The receiving branch 11 of each transmitting/receiving module 3 comprises, in cascade from the relative radiating element 2, a low-noise amplifier (LNA) 14 and an analogue-to-digital converter (ADC). Thus, each radiating element 2 is connected to the output of the relative HPA 13 and to the input of the relative LNA 14. In addition, each transmitting/receiving module 3 comprises a PLL circuit 16 for maintaining synchronism between the DAC 12 and the ADC 15.

The DACs 12 and the ADCs 15, through the relative PLL circuits 16, as well as the signal generation and conversion module 4, sample the reference clock so as to maintain synchronism between them and the processor 5.

The antenna 1 further comprises a digital beam forming network 17, which interfaces the signal generation and conversion module 4 to the processor 5 in the signal reception path and operates in a known manner.

The antenna 1 further comprises a calibration antenna 18, which is arranged in front of the radiating elements 2 so as to illuminate all of them, and comprises its own transmitting module 19 commanded by the processor 5 to perform some steps of the method of the invention, as will be explained in detail hereinafter.

The processor 5 is configured to implement the method of the invention to recover the digital error of the antenna 1 after powering the antenna 1 itself off/on again.

With reference to Figure 3, the method of the invention comprises a plurality of steps to be performed after the calibration of the antenna 1 (step 100), generally groupable into a phase of recording a reception state (step 200) and a phase of recording a transmission state (step 300), and a plurality of steps to be performed after powering off/on again the antenna 1 (step 400), generally groupable into a reception state recovery

phase (step 500) and into a transmission state recovery phase (step 600).

In particular, the reception state recording phase (step 200) comprises, for each radio frequency of the plurality of radio frequencies and for each radiating element 2, the acquisition of a digital state SCalRx relative to said radio frequency in reception, and the recording, i.e. the storage, of the digital state SCalRx in the non-volatile memory 6. The digital state SCalRx comprises a delay and phase, with respect to the reference clock, associated with the radiating element 2 during reception at the specified radio frequency. Adopting an indexed representation, the digital state SCalRx(k,f) comprises the delay and the phase associated with the generic radiating element denoted by k, during reception at the generic radio frequency denoted by f.

In more detail, the acquisition of the digital state SCalRx involves transmitting, via the calibration antenna 18, a signal s(t) consisting of a chirp pulse (t) having an unknown delay and phase, receiving the signal s(t) via each of the transmitting/receiving modules 3, and, for each of the radiating elements 2, obtaining a digital signal u(t) by performing a digital deramping or dechirping of the received signal s(t) and determining the delay and the phase associated with the radiating element 2 based on a digital processing of the signal u(t).

The signal s(t) can be expressed with the following formula:

$$s(t) = exp\left\{j \cdot 2\pi\left(\frac{B}{2T}(t-t_0)^2 - \frac{B}{2}(t-t_0)\right)\right\} \cdot exp\{j \cdot \varphi_0\},$$

wherein, B is the instantaneous chirp band, T is the duration of the chirp pulse, $t_0$ is the unknown delay and $\varphi_0$ is the unknown phase.

The signal s(t) expressed by the formula above is in base or intermediate band and the calibration antenna 18 transmits the corresponding translated signal to the generic radio frequency used to determine the specific digital state.

Deramping the received signal s(t) consists of digitally multiplying the received signal s(t) by a signal d(t) consisting of a complex conjugate copy of the signal s(t), but with known delay and phase, e.g. zero:

$$d(t) = exp\left\{-j \cdot 2\pi\left(\frac{B}{2T}t^2 - \frac{B}{2}t\right)\right\},$$

so as to obtain the signal u(t) expressed as follows:

$$u(t) = exp\left\{-j \cdot 2\pi\frac{B \cdot t_0}{T}t\right\} \cdot exp\left\{j \cdot 2\pi\frac{B}{2}\left(t_0 + \frac{t_0^2}{T}\right)\right\} \cdot exp\{j \cdot \varphi_0\}.$$

Typically, the delays of the radiating elements 2 to be estimated by the method of the invention are of the order of a few periods of the reference clock, i.e. a few nanoseconds. On the other hand, the duration of the chirp pulse T is instead of a few

microseconds. Therefore, it can be assumed that the delay $t_0$ is much lower than the pulse duration T, and consequently the signal u(t) can be approximated as follows:

$$u(t) \cong exp\left\{-j \cdot 2\pi \frac{B \cdot t_0}{T} t\right\} \cdot exp\left\{j \cdot 2\pi \frac{B \cdot t_0}{2}\right\} \cdot exp\{j \cdot \varphi_0\}.$$

The signal u(t) thus obtained consists of a sinusoid expressed in digital form, the argument of which is a linear function of time (straight line):

$$\varphi(t) = -2\pi \frac{Bt_0}{T} t + \pi B t_0 + \varphi_0.$$

It is observed that the slope of the function φ(t) depends on the delay $t_0$ and that the initial value (intercept of ordinates) of the function φ(t) depends on the delay $t_0$ and on the phase $\varphi_0$. Furthermore, in the specific case of acquisition of the digital state SCalRx(k,f), $t_0$ and $\varphi_0$ would represent the delay and, respectively, the phase with respect to the reference clock associated with the radiating element k during reception at radio frequency f. For this reason, the determination of the delay and of the phase associated with the generic radiating element 2 includes the following digital processing of the signal u(t).

The digital signal φ(t) is obtained as the arcsine of the digital signal u(t). The slope and the initial value of the signal φ(t) are estimated by linear regression. The delay associated with the radiating element 2 is calculated as a function of the slope of the signal φ(t), of the instantaneous band B of the signal s(t) and of the duration T of the signal s(t). The phase associated with the radiating element 2 is calculated as a function of the initial value of the signal φ(t), of the delay calculated as above and of the instantaneous band B of the signal s(t).

The transmission state recording phase (step 300) comprises, for each radio frequency of the plurality of radio frequencies and for each radiating element 2, the acquisition of a digital state SCalTx relative to said radio frequency in transmission, and the recording of the digital state SCalTx in the non-volatile memory 6. The digital state SCalTx comprises a delay and a phase, with respect to the reference clock, associated with the radiating element 2 during transmission at the specified radio frequency. With an indexed representation, the digital state SCalTx(k,f) comprises the delay and the phase associated with the generic radiating element denoted by k, during reception at the generic radio frequency denoted by f.

The transmission state recording phase (step 300) differs from the reception state recording phase (step 200) in that in each transmitting/receiving module 3, the respective DAC 12 transmits the signal s(t) directly to the ADC 15. In other words, the DAC 12 is looped over the respective converter ADC 15 so that the signal s(t) transmitted by the

DAC 12 is received directly by the ADC 15.

With particular reference to Figure 2, each transmitting/receiving module 3 comprises a by-pass connection 20 that can be activated by the processor 5 to connect the output of the DAC 12 directly to the input of the ADC 15 for the purpose of by-passing the entire analogue part of the transmitting/receiving module 3, i.e. the two amplifiers HPA 13 and LNA 14 and the radiating element 2.

The signal s(t) is in base or intermediate band and the signal generation and conversion module 4 generates the corresponding translated signal to the radio frequency used, to be applied to the input of the DAC 12.

The reception state recovery phase (step 500) comprises, for a test radio frequency selected from the plurality of radio frequencies and for each radiating element 2, acquiring a digital state SCurRx relative to the test radio frequency in reception and comparing the digital state SCurRx with the digital state SCalRx relative to the test radio frequency to determine a time offset ΔtRx and a phase shift ΔφRx that are associated with the radiating element 2 in reception.

The acquisition of the digital state SCurRx relative to the test radio frequency is performed in the same manner as the acquisition of the digital state SCalRx for a generic radio frequency, described above in relation to the phase of recording a reception state (step 200), i.e. using the calibration antenna 18 to transmit the signal s(t) translated to the test radio frequency.

By adopting an indexed representation, the digital state SCurRx (k) comprises the delay and the phase that are associated with the generic radiating element denoted by k. Thus, for each radiating element denoted by k, the digital state SCurRx(k) is compared with the digital state SCalRx (k,f1) at the test radio frequency denoted by f1.

In particular, the delay $t_{Cur}$ and the phase $\varphi_{Cur}$ of the digital state SCurRx(k) are compared with the delay $t_{Cal}$ and the phase $\varphi_{Cal}$ of the digital state SCalRx(k,f1), respectively. In more detail, said comparison involves calculating a first time difference among the delays $t_{Cur}$ and $t_{Cal}$ and determining the time offset ΔtRx by rounding the first time difference to an integer number of reference clock periods, according to the following formula:

$$\Delta tRx = \frac{round\left((t_{Cur} - t_{Cal}) \cdot f_{ck}\right)}{f_{ck}}$$

wherein $f_{ck}$ is the reference clock frequency and *round()* is the function of rounding to the nearest integer.

Furthermore, said comparison provides for calculating a first phase difference

among the phases $\varphi_{Cur}$ and $\varphi_{Cal}$ and determining the phase shift $\Delta\varphi Rx$ by subtracting from the first phase difference the phase shift introduced by the time offset $\Delta tRx$ at the test radio frequency, according to the following formula:

$$\Delta\varphi Rx = \varphi_{Cur} - \varphi_{Cal} - 2 \cdot \pi \cdot f_{RF} \cdot \Delta tRx$$

wherein $f_{RF}$ is the test radio frequency.

The reception state recovery phase ends with the reconfiguration of the signal generation and conversion module 4 so that the latter applies, to each transmitting/receiving module 3, the relative time offset $\Delta tRx$ and the relative phase shift $\Delta\varphi Rx$ in reception, regardless of the radio frequency of the plurality of radio frequencies that will subsequently be used by the antenna 1. Thus, the time offset $\Delta tRx$ and the phase shift $\Delta\varphi Rx$ of the radiating elements 2 are the compensation coefficients that allow the recovery of the digital states in reception recorded immediately after calibration of the antenna 1 and thus allow the substantial restoration of the equiphase plane condition on the antenna 1.

The transmission state recovery phase (step 600) comprises, for each radiating element 2, acquiring a digital state SCurTx relative to the test radio frequency in transmission and comparing the digital state SCurTx with the digital state SCalTx relative to the test radio frequency to determine a time offset $\Delta tTx$ and a phase shift $\Delta\varphi Tx$ that are associated with the radiating element 2 in transmission. By adopting an indexed representation, the digital state SCurTx(k) comprises the delay and the phase that are associated with the generic radiating element denoted by k. Thus, for each radiating element denoted by k, the digital state SCurTx(k) is compared with the digital state SCalTx(k,f1) at the test radio frequency denoted by f1.

The transmission state recovery phase (step 600) differs from the reception state recovery phase (step 500) in that in each transmitting/receiving module 3, the respective converter DAC 12 transmits the signal s(t) directly to the converter ADC 15, i.e. in that the signal s(t) is transmitted like in the transmission state recording phase, but only for the test radio frequency.

The transmission state recovery phase (step 600) is performed after the reception state recovery phase, and thus the signal generation and conversion digital module 4 is already reconfigured to apply the time offsets $\Delta tRx$ and the phase shifts $\Delta\varphi Rx$ before the signal s(t) is transmitted by the DAC 12. This allows the digital error on the receiving branch 11 to be compensated so that it does not overlap with the digital error on the transmitting branch 10 when determining the digital state SCurTx.

Thus, the time offset ΔtTx and the phase shift ΔφTx are calculated using the following formulas:

$$\Delta tTx = \frac{round\left((t_{Cur} - t_{Cal}) \cdot f_{ck}\right)}{f_{ck}}$$

$$\Delta\varphi Tx = \varphi_{Cur} - \varphi_{Cal} - 2 \cdot \pi \cdot f_{RF} \cdot \Delta tTx$$

wherein $t_{Cur}$ and $\varphi_{Cur}$ are delay and phase of the digital state SCurTx(k) and $t_{Cal}$ and $\varphi_{Cal}$ are delay and phase of the digital state SCalTx(k,f1).

The transmission state recovery phase ends with the reconfiguration of the signal generation and conversion module 4 so that the latter applies, to each transmitting/receiving module 3, the relative time offset ΔtTx and the relative phase shift ΔφTx in transmission, regardless of the radio frequency of the plurality of radio frequencies that will subsequently be used by the antenna 1. Thus, the time offset ΔtTx and the phase shift ΔφTx of the radiating elements 2 are the compensation coefficients that allow the recovery of the digital states in transmission recorded immediately after calibration of the antenna 1 and thus allow the substantial restoration of the equiphase plane condition on the antenna 1.

It is noted that the test radio frequency used for the reception state recovery phase and the transmission state recovery phase is selected on the basis of the electromagnetic situation in which the antenna 1 is when powered on again. In particular, the test radio frequency must not be jammed by external systems.

The method described above for recovering the digital error of a digital array antenna after powering it off/on again drastically reduces the time required to compensate for the phase errors due to clock metastability, compared to a normal antenna calibration. In other words, the method of the invention requires only two measurements, a first one on the test frequency in reception and the second on the test frequency in transmission, as opposed to the 2*Nf measurements of a normal calibration.

In fact, after powering the antenna 1 on again, the current digital state in reception SCurRx and in transmission SCurTx for each radiating element is only acquired again for a single test radio frequency. The current digital state SCurRx and SCurTx is then compared with the recorded digital state SCalRx and SCalTx to determine the compensation coefficients, i.e. the time offsets ΔtRx and ΔtTx and the phase shifts ΔφRx and ΔφTx, which allow the phases of the radiating elements 2 to be corrected for any radio frequency. This is made possible by the fact that the digital state of a radiating element 2 does not change as the radio frequency used varies, so it is sufficient to determine the compensation coefficients for a single radio frequency.

The recording of the digital states of all radiating elements 2 is made for all the radio frequencies usable by antenna 1, as it is not possible to know in advance which test radio frequency will be usable for the recovery of the digital states. In fact, when powering the antenna 1 on again, it is necessary to select as test radio frequency one of the radio frequencies that are not disturbed by external systems at that moment.

## CLAIMS

1. Method for recovering the digital error of a digital array antenna, in particular for a digital array radar, after powering off and on of the digital array antenna, the digital array antenna (1) comprising a plurality of radiating elements (2), a corresponding plurality of transmitting/receiving modules (3) adapted to operate at a plurality of radio frequencies, a signal generation and conversion digital module (4) for generating baseband or intermediate band signals and converting them to and from radio frequency, a processor (5) comprising a non-volatile memory (6) and adapted to control the signal generation and conversion digital module (4), and a reference clock generator (7), the transmitting/receiving modules (3) comprising a transmitting branch (10) and a receiving branch (11), both of which are connected between the relative radiating element (2) and the signal generation and conversion digital module (4), the transmitting branch (10) comprising in cascade towards the relative radiating element (2) a digital-to-analogue converter (12) and a first amplifier (13), and the receiving branch (11) comprising in cascade from the relative radiating element (2) a second amplifier (14) and an analogue-to-digital converter (15); the method comprising:

- immediately after a calibration of the digital array antenna (1), for each radio frequency of the plurality of radio frequencies and for each radiating element (2), acquiring a first digital state (SCalRx) relative to said radio frequency in reception and a second digital state (SCalTx) relative to said radio frequency in transmission, said first and second digital state (SCalRx, SCalTx) each comprising a delay and a phase, with respect to the reference clock, associated with the radiating element (2);
- recording first and second digital state (SCalRx, SCalTx) in non-volatile memory (6);
- after any powering off and on of the digital array antenna (1) occurring after the calibration thereof, for a test radio frequency selected from the plurality of radio frequencies and for each radiating element (2), acquiring a third digital state (SCurRx) relative to the test radio frequency in reception and a fourth digital state (SCurTx) relative to the test radio frequency in transmission, said third and fourth digital states (SCurRx, SCurTx) each comprising a delay and a phase, with respect to the reference clock, associated with the radiating element (2);
- for each radiating element (2), comparing the third digital state (SCurRx) with the first digital state (SCalRx) relative to the test radio frequency to determine a first time offset ($\Delta tRx$) and a first phase shift ($\Delta\varphi Rx$) and comparing the fourth digital state (SCurTx) with the second digital state (SCalTx) relative to the test radio frequency to determine a

second time offset ($\Delta tTx$) and a second phase shift ($\Delta\varphi Tx$); and

- configuring the signal generation and conversion digital module (4) so that the latter applies, to each transmitting/receiving module (3), the relative first time offset ($\Delta tRx$) and first phase shift ($\Delta\varphi Rx$) in reception and the relative second time offset ($\Delta tTx$) and second phase shift ($\Delta\varphi Tx$) in transmission;

the acquisition of the first digital state (SCalRx) and the acquisition of the third digital state (SCurRx) comprising, each:

- transmitting a first signal (s(t)) consisting of a chirp via a calibration antenna (18);
- receiving the first signal (s(t)) via each transmitting/receiving module (3);
- for each radiating element (2), obtaining a second digital signal (u(t)) by performing a digital deramping of the first received signal (s(t)) and determining the delay and the phase associated with the radiating element (2) based on a digital processing of the second signal (u(t));

the acquisition of the second digital state (SCalTx) and the acquisition of the fourth digital state (SCurTx) comprising, each:

- in each transmitting/receiving module (3), transmitting a first signal (s(t)) consisting of a chirp pulse from the digital-to-analogue converter (12) directly to the analogue-to-digital converter (15); and
- for each radiating element (2), obtaining a second signal (u(t)) by performing a deramping of the first received signal (s(t)) and determining the delay and the phase associated with the radiating element (2) based on a digital processing of the second signal (u(t)).

2. Method according to claim 1, wherein the acquisition of the fourth digital state (SCurTx) is performed after the comparison between the third digital state (ScurRx) with the first digital state (ScalRx) relative to the test radio frequency to determine the first time offset and the first phase shift for each radiating element (2), and the transmission of the first signal (s(t)) is carried out after configuring the signal generation and conversion digital module (4) so that the latter applies the relative first time offset ($\Delta tRx$) and first phase shift ($\Delta\varphi Rx$) in reception to each transmitting/receiving module (3).

3. Method according to claim 1, wherein performing a digital deramping of the first received signal (s(t)) comprises:

- digitally multiplying the first received signal (s(t)) by a third signal (d(t)) consisting of a complex conjugate copy of the first signal (s(t)) with known delay and phase, so as to

obtain, as a second signal (u(t)), a signal that can be approximated to a sinusoid.

4. Method according to claim 3, wherein determining the delay and the phase associated with the radiating element (2) comprises:

- obtaining a fourth digital signal (φ(t)) as the arcsine of the second signal (u(t));
- estimating slope and initial value of the fourth signal (φ(t)) by linear regression;
- calculating the delay associated with the radiating element (2) as a function of the slope; and
- calculating the phase associated with the radiating element (2) as a function of the initial value.

5. Method according to any one of claims 1 to 4, wherein comparing the third digital state (SCurRx) with the first digital state (SCalRx) relative to the test radio frequency comprises:

- calculating a first time difference between the delay of the third digital state (SCurRx) and the delay of the first digital state (SCalRx); and
- determining the first time offset (ΔtRx) by rounding the first time difference to an integer number of reference clock periods;

and comparing the fourth digital state (SCurTx) with the second digital state (SCalTx) relative to the test radio frequency comprises:

- calculating a second time difference between the delay of the fourth digital state (SCurTx) and the delay of the second digital state (SCalTx); and
- determining the second time offset (ΔtTx) by rounding the second time difference to an integer number of reference clock periods.

6. Method according to claim 5, wherein comparing the third digital state (SCurRx) with the first digital state (SCalRx) relative to the test radio frequency comprises:

- calculating a first phase difference between the phase of the third digital state (SCurRx) and the phase of the first digital state (SCalRx);
- calculating the first phase shift (ΔφRx) by subtracting from the first phase difference the phase shift introduced by the first time offset (ΔtRx) at the test radio frequency;

and comparing the fourth digital state (SCurTx) with the second digital state (SCalTx) relative to the test radio frequency comprises:

- calculating a second phase difference between the phase of the fourth digital state (SCurTx) and the phase of the second digital state (SCalTx);

- calculating the second phase shift ($\Delta\varphi Tx$) by subtracting from the second phase difference the phase shift introduced by the second time offset ($\Delta tTx$) at the test radio frequency.

7. Digital array antenna, in particular for a digital array radar, comprising a plurality of radiating elements (2), a corresponding plurality of transmitting/receiving modules (3) adapted to operate at a plurality of radio frequencies, a signal generation and conversion digital module (4) for generating baseband signals and converting them to and from radio frequency, a calibration antenna (18) provided with a respective transmitting module (19), a reference clock generator (7), and a processor (5), which comprises a non-volatile memory (6) and is adapted to control the signal generation and conversion digital module (4) and the transmitting module (19) of the calibration antenna (18); the transmitting/receiving modules (3) comprising a transmitting branch (10) and a receiving branch (11), both of which are connected between the relative radiating element (2) and the signal generation and conversion digital module (4), the transmitting branch (10) comprising in cascade towards the relative radiating element (2) a digital-to-analogue converter (12) and a first amplifier (13), and the receiving branch (11) comprising in cascade from the relative radiating element (2) a second amplifier (14) and an analogue-to-digital converter (15); the processor (5) being configured to implement the method according to any one of claims 1 to 6.