CLAIMS

1. A layout method for an integrated circuit, comprising the following steps:

providing a layout, the layout comprising a first element region and a second element region, a spacing region being provided between the first element region and the second element region; and

detecting whether a width of the spacing region is less than a preset width, and if yes, marking at least one of the first element region, the second element region and the spacing region, the preset width being a minimum width meeting a requirement, wherein the requirement is to fill the spacing region with at least one dummy pattern;

wherein the first element region comprises a first active area, a first gate pattern located in the first active area and a first auxiliary pattern located on one side of the first element region toward the second element region, and the second element region comprises a second active area, a second gate pattern located in the second active area and a second auxiliary pattern located on one side of the second element region toward the first element region; and

the step of detecting whether a width of the spacing region is less than a preset width comprises:

measuring a distance between the first auxiliary pattern and the second auxiliary pattern; or

measuring a distance between the first active area and the second active area, and calculating a distance between the first auxiliary pattern and the second auxiliary pattern;

wherein the preset width comprises a first subpreset width and a second subpreset width;

the first subpreset width is a minimum width meeting the requirement and existing between the dummy pattern for filling and the first auxiliary pattern, and the second subpreset width is a minimum width meeting the requirement and existing between the dummy pattern for filling and the second auxiliary pattern; and

the minimum width meeting the requirement and existing between the dummy pattern for filling and the first auxiliary pattern is equal to a distance between the first auxiliary pattern and the first gate pattern, and the minimum width meeting the requirement and existing between the dummy pattern for filling and the second auxiliary

pattern is equal to a distance between the second auxiliary pattern and the second gate pattern.

2. The layout method for an integrated circuit according to claim 1, further comprising the following step:

determining whether the width of the spacing region is less than the preset width, and if no, filling the spacing region with at least one dummy pattern.

3. The layout method for an integrated circuit according to claim 2, wherein the step of filling the spacing region with at least one dummy pattern specifically comprises:

determining whether a line width of the first gate pattern is equal to that of the second gate pattern, and if yes, filling the spacing region with the at least one dummy pattern, a line width of the dummy pattern being equal to that of the first gate pattern or the second gate pattern.

4. The layout method for an integrated circuit according to claim 2, wherein the step of filling the spacing region with at least one dummy pattern specifically comprises:

determining whether a line width of the first gate pattern is equal to that of the second gate pattern, if no, determining whether the width of the spacing region meets a requirement of simultaneous filling of a first dummy pattern and a second dummy pattern, and if yes, simultaneously filling the spacing region with the first dummy pattern and the second dummy pattern, the first dummy pattern being a pattern with a line width the same as the first gate pattern, and the second dummy pattern being a pattern with a line width the same as the second gate pattern.

5. The layout method for an integrated circuit according to claim 2, wherein the step of filling the spacing region with at least one dummy pattern specifically comprises:

determining whether a line width of the first gate pattern is equal to that of the second gate pattern, if no, determining whether the width of the spacing region meets a requirement of simultaneous filling of a first dummy pattern and a second dummy pattern, if no, re-determining whether the line width of the first gate pattern is less than that of the second gate pattern, if yes, filling the spacing region with only the first dummy pattern, and if no, filling the spacing region with only the second dummy pattern, the first dummy

pattern being a pattern with a line width the same as the first gate pattern, and the second dummy pattern being a pattern with a line width the same as the second gate pattern.

6. The layout method for an integrated circuit according to claim 4 or 5, wherein a length of the first dummy pattern is equal to that of the first gate pattern or the first auxiliary pattern, and a length of the second dummy pattern is equal to that of the second gate pattern or the second auxiliary pattern.

7. The layout method for an integrated circuit according to claim 4, further comprising the following step:

determining whether a distance between the first dummy pattern and the second dummy pattern after filling is less than a first threshold, and if yes, enabling the first dummy pattern for filling to be connected to the second dummy pattern for filling.

8. The layout method for an integrated circuit according to claim 1, further comprising the following step:

determining whether a conductive plug adjacent to the first element region exists on a periphery of the first element region, and if yes, filling a space between the first element region and the conductive plug with a plug dummy pattern, a line width of the plug dummy pattern being equal to that of the first gate pattern.

9. The layout method for an integrated circuit according to claim 1, wherein the layout further comprises a conductive plug and a third element region adjacent to the first element region; the third element region comprises a third active area, a third gate pattern located in the third active area and a third auxiliary pattern located on an outer side of the third active area; and the layout method for an integrated circuit further comprises the following step:

determining whether the first element region, the third element region and the conductive plug jointly define a blank region, and if yes, filling the blank region with a third dummy pattern matching both the first element region and the third element region, the blank region being a region provided with no gate pattern.

10. The layout method for an integrated circuit according to claim 9, wherein the first gate pattern and the third gate pattern extend along a first direction, the first gate pattern and

the third gate pattern are spaced along a second direction, the first direction is perpendicular to the second direction, and a length or position of the first gate pattern in the first direction is beyond that of the third gate pattern; and the step of filling the blank region with the third dummy pattern matching both the first element region and the third element region specifically comprises:

filling the blank region with the third dummy pattern extending along the first direction, a position of the third dummy pattern being aligned with that of the third gate pattern or the third auxiliary pattern in the first direction and aligned with that of the first gate pattern or the first auxiliary pattern in the second direction.

11. The layout method for an integrated circuit according to claim 10, wherein the blank region is filled with a plurality of third dummy patterns; and

in the second direction, a distance between adjacent third dummy patterns is equal to that between the third gate pattern and the third auxiliary pattern.

12. The layout method for an integrated circuit according to claim 10, further comprising the following step:

determining whether another element pattern exists in the blank region, and if yes, controlling a minimum distance between the third dummy pattern and the another element pattern is greater than or equal to a second threshold.

13. The layout method for an integrated circuit according to claim 1, after the step of marking at least one of the first element region, the second element region and the spacing region, further comprising the following step:

adjusting a position of the first element region and/or the second element region to increase the width of the spacing region to the preset width.

14. The layout method for an integrated circuit according to claim 1, after the step of marking at least one of the first element region, the second element region and the spacing region, further comprising the following step:

determining whether the width of the spacing region is less than the first subpreset width, and if no, filling the spacing region with the dummy pattern, a line width of the dummy pattern being equal to that of the first gate pattern.

15. The layout method for an integrated circuit according to claim 14, after the width of the spacing region is determined to be greater than the first subpreset width, further comprising the following step:

determining whether a distance between the dummy pattern filling the spacing region and the second auxiliary pattern is less than a first threshold, and if yes, enabling the dummy pattern for filling to be connected to the second auxiliary pattern.

16. A layout apparatus for an integrated circuit, comprising:

a memory module configured to store a layout, the layout comprising a first element region and a second element region, a spacing region being provided between the first element region and the second element region; and

a detection module connected to the memory module and configured to detect whether a width of the spacing region is less than a preset width, and if yes, mark at least one of the first element region, the second element region and the spacing region, the preset width being a minimum width meeting a requirement, wherein the requirement is to fill the spacing region with at least one dummy pattern;

wherein the first element region comprises a first active area, a first gate pattern located in the first active area and a first auxiliary pattern located on one side of the first element region toward the second element region, and the second element region comprises a second active area, a second gate pattern located in the second active area and a second auxiliary pattern located on one side of the second element region toward the first element region; and

the detection module is configured to measure a distance between the first auxiliary pattern and the second auxiliary pattern; or

the detection module is configured to measure a distance between the first active area and the second active area, and calculate a distance between the first auxiliary pattern and the second auxiliary pattern;

wherein the preset width comprises a first subpreset width and a second subpreset width;

the first subpreset width is a minimum width meeting the requirement and existing between the dummy pattern for filling and the first auxiliary pattern, and the second subpreset width is a minimum width meeting the requirement and existing between the dummy pattern for filling and the second auxiliary pattern; and

the minimum width meeting the requirement and existing between the dummy pattern for filling and the first auxiliary pattern is equal to a distance between the first auxiliary pattern and the first gate pattern, and the minimum width meeting the requirement and existing between the dummy pattern for filling and the second auxiliary pattern is equal to a distance between the second auxiliary pattern and the second gate pattern.

17. The layout apparatus for an integrated circuit according to claim 16, further comprising:

a filling module connected to the detection module and configured to fill the spacing region with at least one dummy pattern when the detection module detects that the width of the spacing region is greater than the preset width.