

Description

This invention relates to a digital threshold detection circuit having a hysteresis feature.

In the field of television, considerable efforts have been directed toward developing a digital television receiver wherein the signals are processed by digital circuitry. A motivation for these efforts comes from the fact that the digital television can offer a number of novel features - such as still picture display, multipicture display, direct hookup to a satellite dish amplifier, etc.

There is a continuing desire in the television industry to improve the signal-to-noise ratio (S/N ratio) of the video signals. There are techniques for improving the S/N ratio which take advantage of the fact that video signals are periodic, whereas the noise is aperiodic. Successive addition or signal averaging of the video signals tends to reinforce the periodic signal components, but it tends to cancel out the aperiodic noise components, whereby the S/N ratio is improved. The signal averaging techniques perform well when the television picture is relatively stationary. However, when significant motion is present in the scene, signal averaging causes degradation of the reproduced image - e.g., comet tails.

U. S. patent application, Serial No. 702,612, filed 19 February 1985 (Filing) corresponding to US-A- 4 639 784, published on 27.01.1987, and entitled "VIDEO SIGNAL RECURSIVE FILTER ADAPTIVELY CONTROLLED RESPONSIVE TO THE HISTORY OF IMAGE MOTION", discloses one technique for dealing with the problem of image motion. The Filing apparatus includes a recursive filter wherein current and stored video signals (which are delayed by one frame period) are proportioned and summed as a function of interimage motion to generate noise reduced video signals. The recursive filter includes a motion detector and an auxiliary frame memory for storing the motion signal at the output of the motion detector. A logic device, responsive to the current and stored motion signal, selects predetermined scale factors (e.g., 1, 1/2 and 1/8) for proportioning the current and delayed video signals.

Typically, the motion detector includes a subtracter for subtracting the stored video signal from the incoming video signal to generate a difference signal. The difference signal, which represents frame-to-frame image motion, is applied to a threshold detector for developing a 1-bit motion signal. The motion signal is a logical zero and a logical one depending upon whether or not the difference signal is less than a threshold level. As previously indicated, the motion signal determines the scale factors used for proportioning the current and delayed video signals in noise reduction systems.

A problem with a motion detector without hysteresis is that when the average difference signal is at or near the threshold level, unwanted signal excursions - such as those produced by noise - cause the detector to switch between the output states, thereby resulting in a spurious motion signal. US-A- 4 090 221 discloses a motion detector comprising a threshold apparatus with hysteresis. This threshold apparatus is based on a plurality of threshold circuits and associated digital circuitry.

In accordance with the present invention, a novel digital threshold detector is provided with a hysteresis feature, whereby a definite switching point is achieved without sacrificing noise immunity. The subject digital threshold detector includes a combining means and a threshold device. When an n-bit digital input signal (e.g., 8-bit difference signal) reaches a first threshold value, a 1-bit output signal (e.g., 1-bit motion signal) from the threshold device goes from a logical zero to a logical one. The 1-bit output signal is combined with the n-bit input signal, and the combined input signal is applied to the threshold device to produce a positive hysteresis effect on the output signal. The combination of the output signal with the input signal serves to define a lower, second threshold value when the output signal is a logical one. Thus, once the input signal reaches the first threshold value and triggers a logical one output signal, the input signal has to drop below the lower, second threshold value before the output signal is allowed to go back to a logical zero. Noise not large enough to drive the input signal from near the first threshold value to the lower, second threshold value is prevented from toggling the threshold detector back and forth, thereby achieving noise immunity.

Pursuant to an illustrative embodiment of the present invention, the 1-bit output signal is merged with the n-bit input signal to generate a combined input signal in which the most significant bit (MSB) represents the 1-bit output signal, and the remaining bits represent the n-bit input signal.

According to an alternative embodiment of the present invention, the 1-bit output signal is algebraically added to the n-bit input signal to generate the aforesaid combined input signal.

Illustratively, the threshold device is a read-only-memory (ROM) responsive to the combined input signal, and programmed to define the first and second threshold values respectively.

Pursuant to an alternative implementation, the threshold device comprises a subtracter for subtracting a reference value from the combined input signal to generate a difference signal, in which the sign bit (or the MSB) defines the 1-bit output signal.

IN THE DRAWINGS :

FIGURE 1 illustrates a schematic block diagram of a threshold detector having a hysteresis feature in accordance with the present invention ;

FIGURES 2-5 show alternative embodiments of the FIGURE 1 threshold detector ; and

FIGURE 6 is a graphical representation of the illustrative threshold levels employed in the FIGURE 2 embodiment.

In the exemplary embodiments of the subject invention described hereinbelow, it is assumed that the input signal to be threshold tested is a sequence of 8-bit binary samples of parallel bits occurring synchronously with and at the same rate as a main clock signal. The output signal is a sequence of 1-bit binary samples occurring synchronously with and at the same rate as the 8-bit input signal.

Unless otherwise indicated, it is assumed that the 8-bit input signal samples are in two's complement binary number system. In the two's complement binary number system, the MSB defines the sign of the numbers. When the MSB is a logical zero, the binary number is positive ; when the MSB is a logical one the binary number is negative.

In the drawings, the interconnections between the various blocks are parallel multiwire connections with the number of conductors being indicated by a numeral next to the slash mark.

FIGURE 1 is a block diagram of a digital threshold detector 20 with a hysteresis feature pursuant to this invention. The threshold detector 20 receives the 8-bit input signal on an input terminal 22 and develops the 1-bit output signal on an output terminal 24. The threshold detector 20 consists of a combining means 40 and a threshold device 50. The 1-bit output signal from the threshold device 50 is delayed by one clock cycle and fed back as one of the two inputs to the combining means 40 to provide a hysteresis effect on the output signal. The combining means 40 combines the 8-bit input signal with the delayed, 1-bit output signal to generate a 9-bit combined input signal. The 9-bit combined input signal is fed to the threshold device 50.

In order to synchronize the two inputs to the combining means 40, a pair of latches 30 and 60 are provided. The latches 30 and 60 simultaneously apply the respective samples of the 8-bit input signal and the delayed, 1-bit output signal to terminals 32 and 62 in response to the clock signal (CS). The source of the clock signal CS is indicated by a numeral 34. The latch 60 additionally serves to delay the 1-bit output signal by one clock cycle before it is applied to the terminal 62.

When the value of the 8-bit input signal increases to a first threshold level, the 1-bit output signal of the threshold device 50 changes from a logical zero to a logical one. The logical one output signal from the threshold device 50 is delayed by one clock cycle, and combined (e.g., merged or added) with the 8-bit input signal. The combination of the 8-bit input signal with the delayed, 1-bit output signal serves to define a lower, second threshold level in the manner explained in conjunction with FIGURES 2-5. Thus, once the delayed 1-bit output signal from the threshold device 50 becomes a logical one, the 8-bit input signal must drop below the lower, second threshold level before the output signal of the threshold device can revert back to a logical zero. Noise amplitudes less than the difference between the first threshold level and the second, lower threshold level will not affect the output of the threshold device 50, thereby providing a margin of noise immunity.

FIGURES 2-5 illustrate various alternative implementations of the threshold detector 20. As previously indicated, the 8-bit input signal is assumed to be in two's complement binary number system. In the FIGURE 2 embodiment, the delayed, 1-bit output signal and the 8-bit input signal are concatenated to form a 9-bit combined input signal in which the MSB and the 8 LSB's respectively represent the output signal and input signal. The 9-bit combined input signal defines a 9-bit address codeword and is applied to the address input port read only random access memory (ROM) 52 having 512 (or 2^9) memory locations for storing the respective 1-bit output signal values.

The ROM 52 is programmed to provide a zero output value for all of the 8 LSB address codewords (i.e., the input signal values) occurring between $\pm$ the first threshold level and to provide a one output value for all other 8 LSB address codewords, when the 9th MSB (i.e., the delayed 1-bit output signal) is a logical zero. The ROM 52 is further programmed to provide a zero output value for all of the 8 LSB address codewords defining values between $\pm$ the second threshold level and to provide a one output value for all other 8 LSB address codewords, when the 9th MSB is a logical one. This program, in part, is illustrated in TABLE 1. All of the 8 LSB address codewords which produce zero output states for this example are illustrated in the table.

This table is developed assuming that both the positive and negative 2's complement input signal values will be applied to the ROM 52. If, however, only the magnitudes of the input signal will be included in the input address codewords, the ROM 52 can be halved, and all of the values (memory locations and address values) corresponding to the negative address codewords may be eliminated.

T A B L E 1

	9-BIT ADDRESS		8-BIT	9th MSB=0	9th MSB=1
	9th MSB	8 LSB ADDRESS	DECIMAL EQUIVALENT	ROM OUTPUT	ROM OUTPUT
5	X	0111 1111	+127	1	1
	X	...	...	1	1
10	X	0000 1010	+10	1	1
	X	0000 1001	+ 9	1	1
	X	0000 1000	+ 8	1*	1
15	X	0000 0111	+ 7	0	1
	X	0000 0110	+ 6	0	1
	X	0000 0101	+ 5	0	1**
	X	0000 0100	+ 4	0	0
20	X	0000 0011	+ 3	0	0
	X	0000 0010	+ 2	0	0
	X	0000 0001	+ 1	0	0
25	X	0000 0000	0	0	0
	X	1111 1111	- 1	0	0
	X	1111 1110	- 2	0	0
	X	1111 1101	- 3	0	0
30	X	1111 1100	- 4	0	0
	X	1111 1011	- 5	0	1**
	X	1111 1010	- 6	0	1
35	X	1111 1001	- 7	0	1
	X	1111 1000	- 8	1*	1
	X	1111 0111	- 9	1	1
	X	...	...	1	1
40	X	1000 0000	-128	1	1

*first threshold value (input signal = ± 8)

**second threshold value (input signal = ± 5)

From FIGURE 6 and TABLE 1, it can be seen that the output signal remains a logical zero as long as the input signal is less than the first threshold level 0000 1000 (or 8). When the input signal reaches the first threshold level, the output signal changes to a logical one.

The logical one output signal is delayed for one clock cycle by the latch 60, and the delayed output signal is applied to the combining means 42. The combining means 42 concatenates the delayed, 1-bit output signal with the 8-bit input signal to generate the 9-bit combined input signal, in which the MSB is the delayed, 1-bit output signal. Once the MSB of the 9-bit combined input signal goes to a logical one, it will be seen from FIGURE 6 and TABLE 1 that the input signal must drop below the second threshold level 0000 0101 (or 5) before the output signal can revert back to a logical zero, thereby providing noise immunity. Noise insufficient to drive the input signal below the second, lower threshold level (i.e., 0000 0101 or 5) is not allowed to pass through once the delayed output signal becomes a logical one. It will be seen that the system response is symmetrical about a zero input value.



The actual values of the first and second threshold levels are determined by considerations such as noise immunity and input signal sensitivity. Basically, the higher the difference between the two threshold levels, the greater the noise immunity and the smaller the sensitivity of the threshold detector 20 to the changes in the input signal.

5 **FIGURE 3** illustrates another embodiment of the present invention. In **FIGURE 3**, the 8-bit input signal is applied to one input port of an adder 43' and the delayed, 1-bit output signal is coupled to the LSB position of a second input port thereof. The adder 43' produces a 9-bit output which is applied to the address port of a ROM 53. The 512 x 1-bit ROM 53 is programmed to define a double threshold window which may correspond to **TABLE 1**. The 1-bit output signal from the ROM 53 is delayed by one clock cycle, and added to the 8-bit input signal to provide hysteresis.

10 Adding the delayed, 1-bit output signal to the least significant bit position of the 8-bit input signal raises the address codeword by one unit. Therefore the input signal must go through a transition of at least two units before the output can change states once it has gone through the first threshold value. It will be recognized by those skilled in the art that the 1-bit output signal may be added to a more significant position of the 8-bit input signal (e.g., 3rd LSB position) to generate a larger difference (e.g., 4 levels) between the two threshold levels.

15 **FIGURE 4** represents a still further embodiment of the present invention. The 8-bit input signal in two's complement binary number system is applied to an absolute value determining means 26. The MSB or the sign bit of the absolute values at the output 28 of the absolute value determining means 26, being redundant, is ignored. The 7 LSB's of the absolute values on the terminal 32' are merged with the delayed, 1-bit output signal on the terminal 62', and the resulting 8-bit combined input signal is applied to a ROM 54 with 256 (or 2⁸) memory locations for storing the respective 1-bit output signal values. The 256 x 1-bit ROM 54 in this arrangement is programmed with a single threshold window corresponding to **TABLE 1**, with the 9th MSB = 0.

20 **FIGURE 5** depicts still another variation of the **FIGURE 4** embodiment of the present invention. An adder 45' adds the delayed, 1-bit output signal to the LSB position of the 7-bit input signal on the terminal 32' to generate an 8-bit combined input signal in a manner similar to that shown in **FIGURE 3**. The output of the adder 45' is applied to the minuend terminal of a subtractor 55'. The subtractor 55' subtracts an 8-bit reference or threshold value from the 8-bit combined input signal from the adder 45' to generate an 8-bit difference signal. The MSB (or the sign bit) of the 8-bit difference signal at the output of the subtractor 55' defines the 1-bit output signal. The 1-bit output signal is delayed, and fed back to the adder 45' to provide hysteresis.

25 It will be obvious to people skilled in the art that many other embodiments of the invention can be conceived without departing from the scope thereof. For example, the function of the threshold means can be realized with the help of hardware (i.e., logic gates) instead of a ROM. In addition, the 1-bit output signal may be concatenated at other than the MSB position of the combined input signal (e.g., at the LSB position thereof) with appropriate programming of the ROM. Such alternative arrangements are intended to be covered by the appended claims.

Claims

- 40 1. A digital threshold detector with hysteresis characterised by :
 a threshold means (50) for producing a 1-bit digital output signal (24) having first and second logic states depending upon the value of the digital input signal to said threshold means ; and
 combining means (40) coupled to a source (22) of an n-bit digital input signal and to said threshold means for combining said n-bit input signal with said 1-bit output signal to generate a combined digital input signal for application to said threshold means ; the combination of said n-bit input signal with said 1-bit output signal effectively changing the digital input signal value at which said threshold detector changes output states between a first threshold value and a second threshold value depending upon whether said output signal is in said first or second logic states respectively.
- 45 2. A digital threshold detector as defined in Claim 1 wherein said combining means (40) concatenates said 1-bit output signal with said n-bit input signal to generate an n+1 bit combined input signal.
- 50 3. A digital threshold detector as defined in Claim 1 wherein said threshold means (50) comprises a ROM (52) having an address input port coupled to said combining means (40) and programmed to output said first state for said n-bit input signal having values being less than said first threshold value and to output said second state for input values greater than said first threshold value for said 1-bit signal exhibiting said first state, and further programmed to output said first state for said n-bit input signal values being less than said second threshold value and to output said second state for input values greater than said second threshold value for said 1-bit signal exhibiting said second state.
- 55 4. A digital threshold detector as defined in Claim 1 further including a source (34) of a clock signal occurring



synchronously with and at the same rate as said digital input signal ; said detector additionally having a latch (60) coupled to the output of said threshold means and clocked by said clock signal for supplying said 1-bit output signal to said combining means (60).

5 5. A digital threshold detector as defined in Claim 4 further including another latch (30) coupled between said source (22) of said digital input signal and said combining means.

6. A digital threshold detector as defined in Claim 1 wherein said combining means (40) includes an adder (45') having a first input port coupled to said input signal source and a second input port coupled to receive said 1-bit output signal for adding said 1-bit output signal to a predetermined bit position of said n-bit input signal.

10 7. A digital threshold detector as defined in Claim 6 wherein said 1-bit output signal is added to the LSB position of said input signal.

8. A digital threshold detector as defined in Claim 7 wherein said threshold means comprises a read-only-memory (53) coupled to the output of said adder.

15 9. A digital threshold detector as defined in Claim 1 wherein said digital input signal consists of a sequence of either all positive or all negative n-bit binary samples in two's complement binary number system ; wherein said combining means (42) concatenates said 1-bit output signal with the n-1 LSB's of said input signal to generate an n-bit combined input signal ; wherein said threshold means comprises a read-only-memory (ROM) (52) having 2^n memory locations addressed by said n-bit combined input signal ; wherein the first $2^{n/2}$ memory locations define said first threshold value in response to said output signal having said first logic state ; wherein the remaining $2^{n/2}$ memory locations define said second threshold value in response to said output signal having said second logic state.

20 10. A digital threshold detector as defined in Claim 1 wherein said digital input signal consists of a sequence of either all positive or all negative n-bit binary samples in two's complement binary number system ; wherein said combining means (45) consists of an adder (45') having a first input port coupled to the n-1 LSB's of said input signal and a second input port coupled to receive said 1-bit output signal for adding said 1-bit output signal to a predetermined bit position of said n-1 LSB's of said input signal ; wherein said threshold means (55) comprises a subtractor (55') and a reference value generating means (55'') ; wherein the minuend and subtrahend terminals of said subtractor are respectively coupled to an output of said adder (45') and to said reference value generating means to provide a difference signal including a polarity representative signal defining said 1-bit output signal.

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Patentansprüche

35 1. Digitaler Schwellenwertdetektor mit Hysterese, gekennzeichnet durch :
eine Schwellenwerteinrichtung (50) zum Erzeugen eines digitalen 1-Bit-Ausgangssignales (24) welches einen ersten oder zweiten logischen Zustand entsprechend dem Wert des digitalen Eingangssignales der Schwellenwerteinrichtung annimmt ; und

40 eine Kombiniereinrichtung (40), die mit einer Quelle (22) für ein digitales n-Bit-Eingangssignal und der Schwellenwerteinrichtung gekoppelt ist, um das n-Bit-Eingangssignal mit dem 1-Bit-Ausgangssignal unter Erzeugung eines kombinierten digitalen Eingangssignales zur Zuführung zur Schwellenwerteinrichtung zu erzeugen, wobei die Kombination des n-Bit-Eingangssignales mit dem 1-Bit-Ausgangssignal effektiv den digitalen Eingangssignalwert ändert, bei dem der Schwellenwertdetektor seinen Ausgangszustand zwischen einem ersten Schwellenwert und einem zweiten Schwellenwert in Abhängigkeit davon, ob das Ausgangssignal sich im ersten oder im zweiten logischen Zustand befindet, ändert.

45 2. Digitaler Schwellenwertdetektor nach Anspruch 1, dadurch gekennzeichnet, daß die Kombiniereinrichtung (40) das 1-Bit-Ausgangssignal mit dem n-Bit-Eingangssignal unter Erzeugung eines kombinierten (n+1)-Bit-Eingangssignales verkettet.

50 3. Digitaler Schwellenwertdetektor nach Anspruch 1, dadurch gekennzeichnet, daß die Schwellenwerteinrichtung (50) ein ROM (52) enthält, welches einen mit der Kombiniereinrichtung (40) gekoppelten Adresseingangsanschluß hat und so programmiert ist, daß es den ersten Zustand für das n-Bit-Eingangssignal mit Werten, die kleiner als der erste Schwellenwert sind, und den zweiten Zustand für Eingangswerte, die größer als der erste Schwellenwert ist, für das den ersten Zustand aufweisende 1-Bit-Signal abgibt, und das weiterhin so programmiert ist, daß es den ersten Zustand für Werte des n-Bit-Eingangssignales, die kleiner als der zweite Schwellenwert sind und den zweiten Zustand für Eingangswerte, die größer als der zweite Schwellenwert ist, abgibt, wenn das 1-Bit-Signal den zweiten Zustand aufweist.

55 4. Digitaler Schwellenwertdetektor nach Anspruch 1, dadurch gekennzeichnet, daß er außerdem eine Quelle (34) für ein Taktsignal aufweist, das synchron mit dem digitalen Eingangssignal und mit der gleichen Rate wie dieses auftritt ; daß der Detektor außerdem einen Signalwertspeicher (60) hat, der mit dem Ausgang



der Schwellenwerteinrichtung gekoppelt und durch das Taktsignal getaktet ist, um das 1-Bit-Ausgangssignal an die Kombiniereinrichtung (60) zu liefern.

5 5. Digitaler Schwellenwertdetektor nach Anspruch 4, dadurch gekennzeichnet, daß er einen weiteren Signalwertspeicher (30) enthält, der zwischen die Quelle (22) des digitalen Eingangssignals und die Kombiniereinrichtung gekoppelt ist.

6. Digitaler Schwellenwertdetektor nach Anspruch 1, dadurch gekennzeichnet, daß die Kombiniereinrichtung einen Addierer (45') enthält, der einen mit der Eingangssignalquelle gekoppelten ersten Eingangsanschluß und einen für den Empfang des 1-Bit-Ausgangssignales geschalteten zweiten Eingangsanschluß aufweist, um das 1-Bit-Ausgangssignal zu einer vorgegebenen Bitstelle des n-Bit-Eingangssignals zu addieren.

10 7. Digitaler Schwellenwertdetektor nach Anspruch 6, dadurch gekennzeichnet, daß das 1-Bit-Ausgangssignal zur niedrigsten Stelle des Eingangssignals addiert wird.

8. Digitaler Schwellenwertdetektor nach Anspruch 7, dadurch gekennzeichnet, daß die Schwellenwerteinrichtung einen mit dem Ausgang des Addierers gekoppelten Lesespeicher (53) enthält.

15 9. Digitaler Schwellenwertdetektor nach Anspruch 1, dadurch gekennzeichnet, daß das digitale Eingangssignal aus einer Folge von entweder nur positiven oder nur negativen binären n-Bit-Abtastwerten im binären Zweierkomplement-Zahlensystem besteht; daß die Kombiniereinrichtung das 1-Bit-Ausgangssignal mit den Bits der n-1 niedrigsten Stellen des Eingangssignales verkettet, um ein kombiniertes n-Bit-Eingangssignal zu erzeugen; daß die Schwellenwerteinrichtung einen Lesespeicher (ROM) (52) mit $2^{n/2}$ Speicherplätzen enthält, die durch das kombinierte n-Bit-Eingangssignal adressiert werden, wobei die ersten $2^{n/2}$ Speicherplätze den ersten Schwellenwert in Ansprache auf das den ersten logischen Zustand aufweisende Ausgangssignal definieren; daß die restlichen $2^{n/2}$ Speicherplätze den zweiten Schwellenwert in Ansprache auf das den zweiten logischen Zustand aufweisende Ausgangssignal definieren.

20 10. Digitaler Schwellenwertdetektor nach Anspruch 1, dadurch gekennzeichnet, daß das digitale Eingangssignal aus einer Folge von entweder nur positiven oder entweder nur negativen binären n-Bit-Abtastwerten im binären Zweierkomplement-Zahlensystem besteht; daß die Kombiniereinrichtung (45) aus einem Addierer (45') besteht, die einen mit den n-1 niedrigsten Bits des Eingangssignales gekoppelten ersten Eingangsanschluß und einen für einen Empfang des 1-Bit-Ausgangssignales geschalteten zweiten Eingangsanschluß aufweist, um das 1-Bit-Ausgangssignal zu einer vorgegebenen Bitstelle der n-1 niedrigsten Stellen des Eingangssignales zu addieren; daß die Schwellenwerteinrichtung (45) einen Subtrahierer (55') und eine Referenzwerterzeugungseinrichtung (55'') enthält; daß der Minuend- und der Subtrahend-Anschluß des Subtrahierers mit einem Ausgang des Addierers (45') bzw. der Referenzwerterzeugungseinrichtung gekoppelt sind, um ein Differenzsignal einschließlich eines polaritätsrepräsentativen Signales, welches das 1-Bit-Ausgangssignal definiert, zu liefern.

35

Revendications

1. Un détecteur à seuil numérique à hystérésis, caractérisé par :
un moyen à seuil (50) pour produire un signal de sortie numérique de 1 bit (24) ayant des premier et
40 second états logiques dépendants de la valeur du signal d'entrée numérique audit moyen à seuil ; et
un moyen de combinaison (40) couplé à une source (22) d'un signal d'entrée numérique de n bits et au moyen à seuil pour combiner le signal d'entrée de n bits au signal de sortie de 1 bit pour produire un signal d'entrée numérique combiné pour application au moyen à seuil ; la combinaison du signal d'entrée de n bits au signal de sortie de 1 bit changeant effectivement la valeur du signal d'entrée numérique à laquelle le détecteur à seuil change d'état de sortie entre une première valeur de seuil et une seconde valeur de seuil suivant
45 que le signal de sortie est respectivement au premier état logique ou au second état logique.

2. Un détecteur à seuil numérique selon la revendication 1 où le moyen de combinaison précité (40) lie le signal de sortie de 1 bit précité au signal d'entrée de n bits pour produire un signal d'entrée combiné de n + 1 bits.

50 3. Un détecteur à seuil numérique selon la revendication 1, où le moyen à seuil (50) comprend une ROM (52) ayant une borne d'entrée d'adresses couplée au moyen de combinaison précité (40) et programmée pour produire le premier état précité pour le signal d'entrée de n bits ayant des valeurs moindres que la première valeur de seuil et pour produire le second état précité pour des valeurs d'entrée supérieures à la première valeur de seuil pour le signal de 1 bit présentant ledit premier état, et également programmée pour produire le premier
55 état pour des valeurs du signal d'entrée de n bits inférieures à la seconde valeur de seuil et pour produire le second état pour des valeurs d'entrée supérieures à la seconde valeur de seuil pour le signal de 1 bit présentant le second état.

4. Un détecteur à seuil numérique selon la revendication 1, comprenant de plus une source (34) d'un signal



d'horloge se produisant de façon synchrone avec et à la même fréquence que le signal d'entrée numérique ; ledit détecteur ayant de plus un moyen de maintien (60) couplé à la sortie du moyen de seuil et synchronisé par le signal d'horloge pour appliquer le signal de sortie de 1 bit au moyen de combinaison précité (60).

5 5. Un détecteur à seuil numérique selon la revendication 4, comprenant de plus un autre moyen de maintien (30) couplé entre la source précitée (22) du signal d'entrée numérique et le moyen de combinaison précité.

6. Un détecteur à seuil numérique selon la revendication 1, où le moyen de combinaison précité (40) comprend un additionneur (45') ayant une première borne d'entrée couplée à la source de signal d'entrée précitée et une seconde borne d'entrée couplée pour recevoir le signal de sortie de 1 bit précité pour additionner le signal de sortie de 1 bit à une position de bit prédéterminée du signal d'entrée de n bits précité.

10 7. Un détecteur à seuil numérique selon la revendication 6, où le signal de sortie de 1 bit précité est additionné à la position LSB du signal d'entrée précité.

8. Un détecteur à seuil numérique selon la revendication 7, où le moyen à seuil précité comprend une mémoire morte (53) couplée à la sortie de l'additionneur précité.

15 9. Un détecteur à seuil numérique selon la revendication 1, où le signal d'entrée numérique précité consiste en une séquence d'échantillons binaires de n bits soit tous positifs soit tous négatifs dans le système de numérotation binaire de complément à deux ; où le moyen de combinaison précité (42) lie le signal de sortie de 1 bit précité aux n-1 LSB du signal d'entrée pour produire un signal d'entrée combiné de n bits ; où le moyen à seuil comprend une mémoire morte (ROM) (52) ayant 2^n emplacements mémoires adressés par le signal d'entrée combiné de n bits ; où les premiers $2^{n/2}$ définissent la première valeur de seuil précitée en réponse au signal de sortie ayant le premier état logique précité ; où les $2^{n/2}$ emplacements mémoires restants définissent la seconde valeur de seuil précitée en réponse au signal de sortie ayant le second état logique précité.

20 10. Un détecteur à seuil numérique selon la revendication 1, où le signal d'entrée numérique précité consiste en une séquence d'échantillons binaires de n bits, soit tous positifs, soit tous négatifs, dans le système de numérotation binaire de complément à deux ; où le moyen de combinaison (45) précité consiste en un additionneur (45') ayant une première borne d'entrée couplée aux n-1 LSB du signal d'entrée précité et une seconde borne d'entrée couplée pour recevoir le signal de sortie de 1 bit précité pour additionner le signal de sortie de 1 bit à une position de bit prédéterminée des n-1 LSB du signal d'entrée ; où le moyen à seuil précité (55) comprend un soustracteur (55') et un moyen de production des valeurs de référence (55'') ; où les bornes diminueuse et diminueur dudit soustracteur sont couplées respectivement à une sortie de l'additionneur (45') et audit moyen de production de valeurs de référence pour produire un signal de différence comprenant un signal représentatif de polarité définissant le signal de sortie de 1 bit.

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