FAST ARBITER WITH DECISION STORAGE

ABSTRACT OF THE DISCLOSURE

Improved circuits for implementing various embodiments of high performance arbiters are disclosed. In one embodiment, a late-done arbiter is implemented by combining a late-decision arbiter with a decision storage (or queue) device. In another embodiment, an arbiter implementation that extends the amount of storage available for decisions is disclosed. A decision making device such as a simple arbiter is followed by a decision storage device such as a queue or a first in first out (FIFO) register of any number of stages. The decision storage device following the arbiter allows the arbiter to report each decision as quickly as it can and to start the next decision making cycle.

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