

**INTEGRATED CIRCUIT MEMORY**Abstract of the Disclosure

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A memory (20) for performing read cycles and write cycles has memory cells (30) located at intersections of word lines (32) and bit line pairs (34). A write control circuit (44) receives a write enable signal. The logic state of the write enable signal determines whether memory (20) writes data into, or reads data from, memory (20). Memory (20) includes row address decoding for selecting a word line (32). During a write cycle, a control signal generated by write control circuit (44) and single-sided delay circuit (45) is provided to row predecoder (42). The old row address is latched, and a new address is prevented from selecting a new word line (32) until the write enable signal changes state to begin a read cycle. Controlling word line selection with the write enable signal ensures that bit line equalization occurs before the beginning of a read cycle.

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FIG. 1 accompanies this abstract.