CHIP FREQUENCY MODULATION METHOD AND APPARATUS OF COMPUTING DEVICE, HASH BOARD, COMPUTING DEVICE AND STORAGE MEDIUM

BACKGROUND OF THE INVENTION

[01] 1. Field of the Invention

[02] The invention relates to the technical field of chip frequency modulation of a computing device, and particularly to a chip frequency modulation method and apparatus of a computing device, a hash board, a computing device and a storage medium.

[03] 2. Related Art

[04] Generally, in the computing device for mass data operation, a large number of operational chips are integrated, and due to limitation of manufacturing process of the operational chips, working performances, hash rates and frequencies of different operational chips are different. Meanwhile, the single operational chip is often formed of a plurality of separate cores, and differences such as process variation and voltage drop at different positions of the operational chip also allow actual working performances of the respective cores to be different. With respect to differences of working performances of different operational chips and cores, how to dynamically modulate actual desired frequencies of the operational chips, and set self-adaptive schemes of the respective cores are urgent problems to be solved. Frequencies supplied for each operational chip and core in the current computing device are consistent, so it is impossible to play computing advantages of the core with good performance, and the core with poor performance has influence on the operational performance of the operational chips, thereby influencing the operational performance of the overall computing device.

[05] In addition, the Chinese patent application CN201611169618.6 discloses a series power supply chip and system, a virtual digital mining machine and a server, comprising a regulator circuit connected to the series power supply chips, respectively, and regulating voltages, temperatures or frequencies of the series power supply chips. When regulating the frequencies of the respective series power supply chips, the regulator circuit detects whether a working state of units to be powered in the series power supply chips is normal according to a preset cycle with respect to the series power supply chips, and if the working state of units to be powered is abnormal, improves or reduces working frequencies of the units to be powered in the abnormal working state according to a preset frequency step within the range of a preset frequency. According to a state indicated by a state register of the unit to be powered, whether the working state of the unit to be powered is normal is judged, and the state indicated by the state register includes a voltage state, a temperature state and a working frequency state; or according to feedback data of data sent from the units to be powered to the unit to be powered, whether the working state of the unit to be powered is normal is judged.

[06] In one embodiment disclosed by the Chinese patent application CN201611169618.6, when regulating the frequencies of the respective series power supply chips, the regulator circuit, as a frequency regulator circuit, can particularly detect whether a working state of units to be powered in the series power supply chips is normal through a detector according to a preset cycle with respect to the series power supply chips, and if the working state of units to be powered is abnormal, can particularly improve or reduce working frequencies of the units to be powered in the abnormal working state through a detector according to a preset frequency step within the range of a preset frequency. As can be seen, CN201611169618.6 discloses that the regulator can regulate frequencies of the chips, but only regulate the working frequencies of the chips according to working states

such as whether the units to be powered send and receive data normally, the voltage state, the temperature state and the frequency state, and the frequency regulation mechanism lacks accuracy, and cannot fully play the operational performance of the chips.

[07] To sum up, the prior art obviously has inconveniences and deficiencies in practical use, so it is necessary to make improvement.

SUMMARY OF THE INVENTION

[08] With respect to the above deficiencies, an object of the invention is to provide a chip frequency modulation method and apparatus of a computing device, a hash board, a computing device and a storage medium, which can automatically modulate a frequency corresponding to each core according to the actual computing performance of each core in the operational chip of the computing device, thereby maximizing the computing performance of the cores and improving the operational performance of the operational chip and the overall operational device.

[09] The invention provides a chip frequency modulation method of a computing device, the computing device provided with at least one operational chip, and the operational chip provided with a plurality of cores, comprising steps of:

[010] setting a plurality of working frequencies for the operational chip of the computing device and causing the plurality of cores in the operational chip to work at the respective working frequencies;

[011] analyzing a computing performance indicator of each core at its current working frequency; and

[012] modulating the current working frequency of the core up or down according to the computing performance indicator of the core.

[013] According to the chip frequency modulation method of the invention, the step of setting a plurality of working frequencies for the operational chip of the computing device and causing the plurality of cores in the operational chip to work at the respective working frequencies further comprises:

[014] setting the plurality of working frequencies for the operational chip through a plurality of phase locked loops, the working frequencies and the phase locked loops being in a one-to-one correspondence relationship;

[015] the step of modulating the current working frequency of the core up or down according to the computing performance indicator of the core further comprises:

[016] modulating the current working frequency of the core up or down through the phase locked loops according to the computing performance indicator of the core.

[017] According to the chip frequency modulation method of the invention, the phase locked loops are provided inside or outside the operational chip.

[018] According to the chip frequency modulation method of the invention, a frequency difference between the adjacent working frequencies is from 1% to 10%.

[019] According to the chip frequency modulation method of the invention, the step of analyzing a computing performance indicator of each core at its current working frequency further comprises:

[020] analyzing whether the computing performance indicator of the core reaches predetermined first, second and/or third indicator thresholds within a predetermined modulation period, the first indicator threshold being the same as or different from the second indicator threshold;

[021] the step of modulating the current working frequency of the core up or down according to the computing performance indicator of the core further comprises:

[022] if the computing performance indicator of the core reaches the first indicator threshold, modulating the current working frequency of the core up to the upper working frequency;

[023] if the computing performance indicator of the core does not reach the second indicator threshold, modulating the current working frequency of the core down to the lower working frequency; and/or

[024] if the computing performance indicator of the core reaches the third indicator threshold, modulating the current working frequency of the core down to the lower working frequency.

[025] According to the chip frequency modulation method of the invention, it further comprises:

[026] if the cores worked at the predetermined at least one optimized working frequency exceed a predetermined first ratio, stopping modulating the frequencies of the cores; or

[027] if the number of cores worked at the at least one optimized working frequency is maximum, stopping modulating the frequencies of the cores.

[028] According to the chip frequency modulation method of the invention, the step of analyzing a computing performance indicator of each core at its current working frequency further comprises:

[029] analyzing whether a computing correct ratio of the core reaches predetermined first and/or second correct ratio thresholds within a predetermined modulation period, the first correct ratio threshold being the same or different from the second correct ratio threshold;

[030] the step of modulating the current working frequency of the core up or down according to the computing performance indicator of the core further comprises:

[031] if the computing correct ratio of the core reaches the first correct ratio threshold, modulating the current working frequency of the core up to the upper working frequency; and/or

[032] if the computing correct ratio of the core does not reach the second correct ratio threshold, modulating the current working frequency of the core down to the lower working frequency.

[033] According to the chip frequency modulation method of the invention, the step of analyzing whether a computing correct ratio of the core reaches predetermined first and/or second correct ratio thresholds within a predetermined modulation period further comprises:

[034] analyzing whether random numbers submitted by the core are correct within the modulation period;

[035] counting the number of correct random numbers and the number of wrong random numbers of the core within the modulation period;

[036] computing a computing correct ratio of the random numbers of the core within the modulation period according to the number of correct random numbers and the number of wrong random numbers, and judging whether the computing correct ratio of the random numbers reaches the predetermined first and/or second correct ratio thresholds;

[037] the step of modulating the current working frequency of the core up or down according to the computing performance indicator of the core further comprises:

[038] if the computing correct ratio of the random numbers of the core reaches the first correct ratio threshold, modulating the current working frequency of the core up to the upper working frequency; and/or

[039] if the computing correct ratio of the random numbers of the core does not reach the second correct ratio threshold, modulating the current working frequency of the core down to the lower working frequency.

[040] According to the chip frequency modulation method of the invention, the step of analyzing whether random numbers submitted by the core are correct within the modulation period further comprises:

[041] computing, via the core, a first result from the random numbers through a predetermined algorithm every time when the core submits one random number within the modulation period, the first result including a first feature;

[042] computing, via a verification unit of the operational chip, a second result from the random numbers through the same algorithm, the second result including a second feature;

[043] if the first feature is the same as the second feature, judging, via the verification unit, that the random numbers are the correct random numbers, or the random numbers are the wrong random numbers.

[044] According to the chip frequency modulation method of the invention, the step of analyzing whether a computing correct ratio of the core reaches predetermined correct ratio thresholds within a predetermined modulation period further comprises:

[045] real-time analyzing whether the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a preset real-time modulating instruction;

[046] analyzing whether the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a preset timed modulating instruction within a modulation time period set by the timed modulating instruction; or

[047] analyzing whether the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a received immediate modulating instruction;

[048] the step of modulating the current working frequency of the core up or down according to the computing performance indicator of the core further comprises:

[049] if the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold, real-time modulating the current working frequency of the core up to the upper working frequency; if the computing correct ratio of the core within the modulation period does not reach the second correct ratio threshold, real-time modulating the current working frequency of the core down to the lower working frequency;

[050] if the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold in the modulation time period, modulating the current working frequency of the core up to the upper working frequency; if the computing correct ratio of the core within the modulation period does not reach the second correct ratio threshold in the modulation time period, modulating the current working frequency of the core down to the lower working frequency; or

[051] according to the received immediate modulating instruction, if the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold, modulating the current working frequency of the core up to the upper working frequency; if the computing correct ratio of the core within the modulation period does not reach the second correct ratio threshold, modulating the current working frequency of the core down to the lower working frequency; according to a received stop modulating instruction, stopping modulating the current working frequency of the core.

[052] According to the chip frequency modulation method of the invention, the step of analyzing a computing performance indicator of each core at its current working frequency further comprises:

[053] presetting a reference node value, a computing correct weight value, a computing wrong weight value, a computing correct threshold and a computing wrong threshold of the core;

[054] analyzing whether each computation of the core is correct;

[055] adding one computing correct weight value to the reference node value every time when the core computes correctly at least once, and reducing one computing wrong weight value from the reference node value every time when the core computes wrongly at least once;

[056] judging whether the current reference node value of the core reaches the computing correct threshold or the computing wrong threshold;

[057] the step of modulating the current working frequency of the core up or down according to the computing performance indicator of the core further comprises:

[058] if the current reference node value of the core reaches the computing correct threshold, modulating the current working frequency of the core up to the upper working frequency;

[059] if the current reference node value of the core reaches the computing wrong threshold, modulating the current working frequency of the core down to the lower working frequency.

[060] According to the chip frequency modulation method of the invention, the step of analyzing whether each computation of the core is correct further comprises:

[061] analyzing whether the random numbers submitted every time by the core are correct;

[062] the step of adding one computing correct weight value to the reference node value every time when the core computes correctly at least once, and reducing one computing wrong weight value from the reference node value every time when the core computes wrongly at least once further comprises:

[063] adding one computing correct weight value to the reference node value every time when the core submits at least one correct random number, and reducing one computing wrong weight value from the reference node value every time when the core submits at least one wrong random number.

[064] According to the chip frequency modulation method of the invention, the step of analyzing whether the random numbers submitted every time by the core are correct further comprises:

[065] computing, via the core, a first result from the random numbers through a predetermined algorithm after the core submits one random number, the first result including a first feature;

[066] computing, via a verification unit of the operational chip, a second result from the random numbers through the same algorithm, the second result including a second feature;

[067] if the first feature is the same as the second feature, judging, via the verification unit, that the random numbers are the correct random numbers, or the random numbers are the wrong random numbers.

[068] According to the chip frequency modulation method of the invention, the method further comprises:

[069] setting and adjusting the reference node value, the computing correct weight value, the computing wrong weight value, the computing correct threshold and/or the computing wrong threshold of the core according to actual requirements, the computing

correct weight value being the same as or different from the computing wrong weight value, the computing correct threshold being the same as or different from the computing wrong threshold;

[070] controlling an expected tolerant resident error ratio of the core by controlling a ratio of the computing correct weight value to the computing wrong weight value;

[071] controlling a modulation period by controlling an absolute value of the computing correct weight value and the computing wrong weight value;

[072] controlling the modulation period by controlling an absolute value of the computing correct threshold and the computing wrong threshold.

[073] According to the chip frequency modulation method of the invention, a computing formula of the resident error ratio is: the resident error ratio = the computing correct weight value divided by the computing correct weight value and the computing wrong weight value.

[074] According to the chip frequency modulation method of the invention, the step of judging whether the current reference node value of the core reaches the computing correct threshold or the computing wrong threshold further comprises:

[075] real-time judging whether the current reference node value of the core reaches the computing correct threshold or the computing wrong threshold according to a preset real-time modulating instruction;

[076] judging whether the current reference node value of the core reaches the computing correct threshold or the computing wrong threshold according to a preset timed modulating instruction within a modulation time period set by the timed modulating instruction; or

[077] analyzing whether the current reference node value of the core reaches the computing correct threshold or the computing wrong threshold according to a received immediate modulating instruction;

[078] the step of modulating the current working frequency of the core up or down according to the computing performance indicator of the core further comprises:

[079] if the current reference node value of the core reaches the computing correct threshold, real-time modulating the current working frequency of the core up to the upper working frequency; if the current reference node value of the core reaches the computing wrong threshold, real-time modulating the current working frequency of the core down to the lower working frequency;

[080] if the current reference node value of the core reaches the computing correct threshold in the modulation time period, modulating the current working frequency of the core up to the upper working frequency; if the current reference node value of the core reaches the computing wrong threshold in the modulation time period, modulating the current working frequency of the core down to the lower working frequency; or

[081] according to the received immediate modulating instruction, if the current reference node value of the core reaches the computing correct threshold, modulating the current working frequency of the core up to the upper working frequency; if the current reference node value of the core reaches the computing wrong threshold, modulating the current working frequency of the core down to the lower working frequency; according to a received stop modulating instruction, stopping modulating the current working frequency of the core.

[082] According to the chip frequency modulation method of the invention, after the step of modulating the current working frequency of the core up or down according to the computing performance indicator of the core, the method further comprises:

[083] counting current distribution state of the cores after frequency modulation at the respective working frequencies;

[084] modulating a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism of the cores, the frequency modulation mechanism being a correspondence relationship between the distribution state and the frequency modulation of the cores.

[085] According to the chip frequency modulation method of the invention, the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency;

[086] the step of modulating a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism of the cores further comprises:

[087] if the cores exceeding a predetermined second ratio are worked at the at least one high-frequency working frequency, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

[088] if the cores exceeding a predetermined third ratio are worked at the at least one low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

[089] According to the chip frequency modulation method of the invention, the step of if the cores exceeding a predetermined second ratio are worked at the at least one high-frequency working frequency, modifying the at least one working frequency to at least one optimized high-frequency working frequency further comprises:

[090] if the cores exceeding the second ratio are worked at the maximum working frequency, modifying the one working frequency to the one optimized high-frequency working frequency; and/or

[091] the step of if the cores exceeding a predetermined third ratio are worked at the at least one low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency further comprises:

[092] if the cores exceeding the third ratio are worked at the minimum working frequency, modifying the one working frequency to the one optimized low-frequency working frequency.

[093] According to the chip frequency modulation method of the invention, the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency;

[094] the step of modulating a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism further comprises:

[095] if the number of cores worked at the at least one high-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency

working frequency being higher than a frequency in the maximum working frequency; and/or

[096] if the number of cores worked at the at least one low-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

[097] According to the chip frequency modulation method of the invention, the step of if the number of cores worked at the at least one high-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized high-frequency working frequency further comprises:

[098] if the number of cores worked at the maximum working frequency is maximum, modifying the one working frequency to the one optimized high-frequency working frequency; and/or

[099] the step of if the number of cores worked at the at least one low-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized low-frequency working frequency further comprises:

[0100] if the number of cores worked at the minimum working frequency is maximum, modifying the one working frequency to the one optimized low-frequency working frequency.

[0101] According to the chip frequency modulation method of the invention, the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency;

[0102] the step of modulating a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism further comprises:

[0103] if the cores exceeding a predetermined fourth ratio are worked at the at least one middle working frequency, stopping modulating the frequency in the working frequency; or

[0104] if the number of cores worked at the at least one middle working frequency is maximum, stopping modulating the frequency in the working frequency.

[0105] According to the chip frequency modulation method of the invention, the computing device is configured to operation of mining virtual digital currency.

[0106] The invention further provides a chip frequency modulation apparatus of a computing device, the computing device provided with at least one operational chip, and the operational chip provided with a plurality of cores, comprising:

[0107] a frequency setting module for setting a plurality of working frequencies for the operational chip of the computing device and causing the plurality of cores in the operational chip to work at the respective working frequencies;

[0108] a computational performance analysis module for analyzing a computing performance indicator of each core at its current working frequency; and

[0109] a frequency modulation module for modulating the current working frequency of the core up or down according to the computing performance indicator of the core.

[0110] According to the chip frequency modulation apparatus of the invention, the frequency setting module sets the plurality of working frequencies for the operational chip through a plurality of phase locked loops, the working frequencies and the phase locked loops being in a one-to-one correspondence relationship;

[0111] the frequency modulation module modulates the current working frequency of the core up or down through the phase locked loops according to the computing performance indicator of the core.

[0112] According to the chip frequency modulation apparatus of the invention, the phase locked loops are provided inside or outside the operational chip.

[0113] According to the chip frequency modulation apparatus of the invention, a frequency difference between the adjacent working frequencies is from 1% to 10%.

[0114] According to the chip frequency modulation apparatus of the invention, the computational performance analysis module analyzes whether the computing performance indicator of the core reaches predetermined first, second and/or third indicator thresholds within a predetermined modulation period, the first indicator threshold being the same as or different from the second indicator threshold;

[0115] if the computing performance indicator of the core reaches the first indicator threshold, the frequency modulation module modulates the current working frequency of the core up to the upper working frequency;

[0116] if the computing performance indicator of the core does not reach the second indicator threshold, the frequency modulation module modulates the current working frequency of the core down to the lower working frequency; and/or

[0117] if the computing performance indicator of the core reaches the third indicator threshold, the frequency modulation module modulates the current working frequency of the core down to the lower working frequency.

[0118] According to the chip frequency modulation apparatus of the invention, the frequency modulation module further comprises:

[0119] a frequency modulation sub-module for modulating the current working frequency of the core up or down according to the computing performance indicator of the core;

[0120] a stop frequency modulation sub-module for if the cores worked at the predetermined at least one optimized working frequency exceed a predetermined first ratio,

stopping modulating the frequencies of the cores; or if the number of cores worked at the at least one optimized working frequency is maximum, stopping modulating the frequencies of the cores.

[0121] According to the chip frequency modulation apparatus of the invention, the computational performance analysis module analyzes whether a computing correct ratio of the core reaches predetermined first and/or second correct ratio thresholds within a predetermined modulation period, the first correct ratio threshold being the same or different from the second correct ratio threshold;

[0122] the frequency modulation module, if the computing correct ratio of the core reaches the first correct ratio threshold, modulates the current working frequency of the core up to the upper working frequency; and/or if the computing correct ratio of the core does not reach the second correct ratio threshold, modulates the current working frequency of the core down to the lower working frequency.

[0123] According to the chip frequency modulation apparatus of the invention, the computational performance analysis module further comprises:

[0124] a first analysis sub-module for analyzing whether random numbers submitted by the core are correct within the modulation period;

[0125] a counting sub-module for counting the number of correct random numbers and the number of wrong random numbers of the core within the modulation period; and

[0126] a first judgment module for computing a computing correct ratio of the random numbers of the core within the modulation period according to the number of correct random numbers and the number of wrong random numbers, and judging whether the computing correct ratio of the random numbers reaches the predetermined first and/or second correct ratio thresholds;

[0127] the frequency modulation module for if the computing correct ratio of the random numbers of the core reaches the first correct ratio threshold, modulating the current working frequency of the core up to the upper working frequency; and/or if the computing correct ratio of the random numbers of the core does not reach the second correct ratio threshold, modulating the current working frequency of the core down to the lower working frequency.

[0128] According to the chip frequency modulation apparatus of the invention, the first analysis sub-module further comprises:

[0129] a first computing unit for computing a first result from the random numbers through a predetermined algorithm every time when the core submits one random number within the modulation period, the first result including a first feature, the first computing unit provided in the core; and

[0130] a first verification unit for computing a second result from the random numbers through the same algorithm, the second result including a second feature, if the first feature is the same as the second feature, judging that the random number is the correct random number, or the random number is the wrong random number, the first verification unit provided in the operational chip.

[0131] According to the chip frequency modulation apparatus of the invention, the computational performance analysis module real-time analyzes whether the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a preset real-time modulating instruction;

[0132] the computational performance analysis module analyzes whether the computing correct ratio of the core within the modulation period reaches the first correct

ratio threshold and the second correct ratio threshold according to a preset timed modulating instruction within a modulation time period set by the timed modulating instruction; or

[0133] the computational performance analysis module analyzes whether the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold and the second correct ratio threshold according to a received immediate modulating instruction;

[0134] the frequency modulation module, if the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold, real-time modulates the current working frequency of the core up to the upper working frequency; if the computing correct ratio of the core within the modulation period does not reach the second correct ratio threshold, real-time modulates the current working frequency of the core down to the lower working frequency;

[0135] the frequency modulation module, if the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold in the modulation time period, modulates the current working frequency of the core up to the upper working frequency; if the computing correct ratio of the core within the modulation period does not reach the second correct ratio threshold in the modulation time period, modulates the current working frequency of the core down to the lower working frequency; or

[0136] the frequency modulation module, according to the received immediate modulating instruction, if the computing correct ratio of the core within the modulation period reaches the first correct ratio threshold, modulates the current working frequency of the core up to the upper working frequency; if the computing correct ratio of the core within the modulation period does not reach the second correct ratio threshold, modulates the current working frequency of the core down to the lower working frequency; according to a

received stop modulating instruction, stops modulating the current working frequency of the core.

[0137] According to the chip frequency modulation apparatus of the invention, the computational performance analysis module further comprises:

[0138] a setting sub-module for presetting a reference node value, a computing correct weight value, a computing wrong weight value, a computing correct threshold and a computing wrong threshold of the core;

[0139] a second analysis sub-module for analyzing whether each computation of the core is correct;

[0140] a counting sub-module for adding one computing correct weight value to the reference node value every time when the core computes correctly at least once, and reducing one computing wrong weight value from the reference node value every time when the core computes wrongly at least once; and

[0141] a second judgment sub-module for judging whether the current reference node value of the core reaches the computing correct threshold or the computing wrong threshold;

[0142] the frequency modulation module for if the current reference node value of the core reaches the computing correct threshold, modulating the current working frequency of the core up to the upper working frequency; and if the current reference node value of the core reaches the computing wrong threshold, modulating the current working frequency of the core down to the lower working frequency.

[0143] According to the chip frequency modulation apparatus of the invention, the second analysis sub-module analyzes whether the random numbers submitted every time by the core are correct;

[0144] the counting sub-module adds one computing correct weight value to the reference node value every time when the core submits at least one correct random number, and reduces one computing wrong weight value from the reference node value every time when the core submits at least one wrong random number.

[0145] According to the chip frequency modulation apparatus of the invention, the second analysis sub-module further comprises:

[0146] a second computing unit for computing, via the core, a first result from the random number through a predetermined algorithm after the core submits one random number, the first result including a first feature; and

[0147] a second verification unit for computing a second result from the random number through the same algorithm, the second result including a second feature; if the first feature is the same as the second feature, judging that the random number is the correct random number, or the random number is the wrong random number.

[0148] According to the chip frequency modulation apparatus of the invention, the setting sub-module sets and adjusts the reference node value, the computing correct weight value, the computing wrong weight value, the computing correct threshold and/or the computing wrong threshold of the core according to actual requirements, the computing correct weight value being the same as or different from the computing wrong weight value, the computing correct threshold being the same as or different from the computing wrong threshold;

[0149] the setting sub-module controls an expected tolerant resident error ratio of the core by controlling a ratio of the computing correct weight value to the computing wrong weight value;

[0150] the setting sub-module controls a modulation period by controlling an absolute value of the computing correct weight value and the computing wrong weight value;

[0151] the setting sub-module controls the modulation period by controlling an absolute value of the computing correct threshold and the computing wrong threshold.

[0152] According to the chip frequency modulation apparatus of the invention, a computing formula of the resident error ratio is: the resident error ratio = the computing correct weight value divided by the computing correct weight value and the computing wrong weight value.

[0153] According to the chip frequency modulation apparatus of the invention, the computational performance analysis module real-time judges whether the current reference node value of the core reaches the computing correct threshold or the computing wrong threshold according to a preset real-time modulating instruction;

[0154] the computational performance analysis module judges whether the current reference node value of the core reaches the computing correct threshold or the computing wrong threshold according to a preset timed modulating instruction within a modulation time period set by the timed modulating instruction; or

[0155] the computational performance analysis module analyzes whether the current reference node value of the core reaches the computing correct threshold or the computing wrong threshold according to a received immediate modulating instruction;

[0156] the frequency modulation module, if the current reference node value of the core reaches the computing correct threshold, real-time modulates the current working frequency of the core up to the upper working frequency; if the current reference node value of the core reaches the computing wrong threshold, real-time modulates the current working frequency of the core down to the lower working frequency;

[0157] the frequency modulation module, if the current reference node value of the core reaches the computing correct threshold in the modulation time period, modulates the current working frequency of the core up to the upper working frequency; if the current reference node value of the core reaches the computing wrong threshold in the modulation time period, modulates the current working frequency of the core down to the lower working frequency; or

[0158] the frequency modulation module, according to the received immediate modulating instruction, if the current reference node value of the core reaches the computing correct threshold, modulates the current working frequency of the core up to the upper working frequency; if the current reference node value of the core reaches the computing wrong threshold, modulates the current working frequency of the core down to the lower working frequency; according to a received stop modulating instruction, stops modulating the current working frequency of the core.

[0159] According to the chip frequency modulation apparatus of the invention, the apparatus further comprises:

[0160] a frequency counting module for counting current distribution state of the cores after frequency modulation at the respective working frequencies;

[0161] a frequency modulation module for modulating a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism of the cores, the frequency modulation mechanism being a correspondence relationship between the distribution state and the frequency modulation of the cores.

[0162] According to the chip frequency modulation apparatus of the invention, the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum

frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency;

[0163] the frequency modulation module further comprises:

[0164] a first frequency modulation sub-module for if the cores exceeding a predetermined second ratio are worked at the at least one high-frequency working frequency, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

[0165] a second frequency modulation sub-module for if the cores exceeding a predetermined third ratio are worked at the at least one low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

[0166] According to the chip frequency modulation apparatus of the invention, if the cores exceeding the second ratio are worked at the maximum working frequency, the first frequency modulation sub-module modifies the one working frequency to the one optimized high-frequency working frequency; and/or

[0167] if the cores exceeding the third ratio are worked at the minimum working frequency, the second frequency modulation sub-module modifies the one working frequency to the one optimized low-frequency working frequency.

[0168] According to the chip frequency modulation apparatus of the invention, the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the

minimum frequency in the low-frequency working frequency is a minimum working frequency;

[0169] the frequency modulation module further comprises:

[0170] a third frequency modulation sub-module for if the number of cores worked at the at least one high-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

[0171] a fourth frequency modulation sub-module for if the number of cores worked at the at least one low-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

[0172] According to the chip frequency modulation apparatus of the invention, if the number of cores worked at the maximum working frequency is maximum, the third frequency modulation sub-module modifies the one working frequency to the one optimized high-frequency working frequency; and/or

[0173] if the number of cores worked at the minimum working frequency is maximum, the fourth frequency modulation sub-module modifies the one working frequency to the one optimized low-frequency working frequency.

[0174] According to the chip frequency modulation apparatus of the invention, the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency;

[0175] the frequency modulation module further comprises:

[0176] a first stop modulation module for if the cores exceeding a predetermined fourth ratio are worked at the at least one middle working frequency, stopping modulating the frequency in the working frequency; or

[0177] a second stop modulation module for if the number of cores worked at the at least one middle working frequency is maximum, stopping modulating the frequency in the working frequency.

[0178] According to the chip frequency modulation apparatus of the invention, the chip frequency modulation apparatus is provided inside or outside the operational chip.

[0179] According to the chip frequency modulation apparatus of the invention, the computing device is configured to operation of mining virtual digital currency.

[0180] The invention further provides a hash board comprising any one of the chip frequency modulation apparatus.

[0181] The invention further provides a computing device comprising any one of the chip frequency modulation apparatus.

[0182] The invention further provides a computer program storage medium for storing a computer program, wherein when executed by a processor, the program implements a chip frequency modulation method of a computing device, the computing device provided with at least one operational chip, and the operational chip provided with a plurality of cores, wherein the method comprises:

[0183] setting a plurality of working frequencies for the operational chip of the computing device and causing the plurality of cores in the operational chip to work at the respective working frequencies;

[0184] analyzing a computing performance indicator of each core at its current working frequency; and

[0185] modulating the current working frequency of the core up or down according to the computing performance indicator of the core.

[0186] The invention automatically modulates frequencies of the cores of the operational chip of the computing device, firstly sets a plurality of suitable working frequencies and causes the plurality of cores in the operational chip to work at the respective working frequencies, and then modulates the current working frequency of the core up or down according to the computing performance indicator of each core at the current working frequency, that is, modulating the core with high computing performance up, and modulating the core with low computing performance down. Therefore, the invention can automatically modulate a frequency corresponding to each core according to the actual computing performance of each core in the operational chip of the computing device, thereby maximizing the computing performance of the cores and improving the operational performance of the operational chip and the overall operational device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0187] FIG. 1 is a structural diagram of a chip frequency modulation apparatus of a computing device according to the invention.

[0188] FIG. 2 is a structural diagram of a chip frequency modulation apparatus of a computing device in a first embodiment of the invention.

[0189] FIG. 3 is a structural diagram of a chip frequency modulation apparatus of a computing device in a second embodiment of the invention.

[0190] FIG. 4 is a structural diagram of a chip frequency modulation apparatus of a computing device in a third embodiment of the invention.

[0191] FIG. 5 is an exemplary diagram of parameter settings in the third embodiment of the invention.

[0192] FIG. 6 is a structural diagram of a chip frequency modulation apparatus of a computing device in a fourth embodiment of the invention.

[0193] FIG. 7 is a distribution state diagram of cores worked at respective working frequencies in the fourth embodiment of the invention.

[0194] FIG. 8 is a flow diagram of a chip frequency modulation method of a computing device according to the invention.

[0195] FIG. 9 is a flow diagram of a chip frequency modulation method of a computing device in the first embodiment of the invention.

[0196] FIG. 10 is a flow diagram of a chip frequency modulation method of a computing device in the second embodiment of the invention.

[0197] FIG. 11 is a flow diagram of a preferable chip frequency modulation method of a computing device in the second embodiment of the invention.

[0198] FIG. 12 is a flow diagram of a chip frequency modulation method of a computing device in the third embodiment of the invention.

[0199] FIG. 13 is a flow diagram of a preferable chip frequency modulation method of a computing device in the third embodiment of the invention.

[0200] FIG. 14 is a flow diagram of a chip frequency modulation method of a computing device in the fourth embodiment of the invention.

[0201] FIG. 15 is a flow diagram one of a preferable chip frequency modulation method of a computing device in the fourth embodiment of the invention.

[0202] FIG. 16 is a flow diagram two of a preferable chip frequency modulation method of a computing device in the fourth embodiment of the invention.

[0203] FIG. 17 is a structural diagram of a computing device according to the invention.

PREFERABLE EMBODIMENTS OF THE INVENTION

[0204] This invention is hereinafter further described in details with reference to the accompanying drawings as well as the embodiments so as to make the object, technical solution and advantages thereof more apparent. It shall be understood that the detailed embodiments described herein are only to explain the invention, instead of limiting the invention.

[0205] It shall be noted that citations of "one embodiment", "embodiments", "an exemplary embodiment" and the like in the disclosure refer to that this embodiment may include specific features, structures or characteristics, but it is unnecessary for each embodiment to include these specific features, structures or characteristics. In addition, such expression does not refer to the same embodiment. Further, with reference to the specific features, structures or characteristics described in this embodiment, no matter whether clear descriptions are made or not, it has shown that combining the specific features, structures or characteristics into other embodiments falls into the knowledge range of those skilled in the art.

[0206] In addition, specific terms are used in the specification and the subsequent claims to refer to specific components or parts. Those skilled in the art shall understand that the manufacturer may give a different name to the same component or part. The specification and the subsequent claims distinguish components or parts from each other by different functions of the components, instead of different names. "Comprise" and "include" mentioned in the whole specification and the subsequent claims are open words, and shall be explained as "include but is not limited to". In addition, "connection" herein includes any direct or indirect electrical connection means. Indirect electrical connection means comprises connection through other devices.

[0207] FIG. 1 is a structural diagram of a chip frequency modulation apparatus of a computing device according to the invention. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. The computing device is provided with at least one operational chip, and the operational chip is provided with a plurality of cores 80. Preferably, the computing device comprises a control board, and a hash board connected to the control board, the hash board is provided with at least one operational chip, and the operational chip is provided with a plurality of cores 80. Of course, the computing device also can comprise a radiator, a connection plate, a power module, and the like.

[0208] It shall be noted that chip frequency modulation technique of the invention actually relates to two levels of frequency modulation mechanism, i.e., a frequency modulation mechanism of the operational chip, and a frequency modulation mechanism on a level of the cores. The frequency modulation mechanism of the operational chip refers to setting a plurality of suitable working frequencies for each operational chip, and causing the respective cores 80 of the operational chip to work at the respective working frequencies, thereby fully play working performance of each core 80. The frequency modulation mechanism on a level of the cores refers to modulating the cores 80 to suitable working frequencies according to the actual computing performance of the core 80, modulating the frequency of the core 80 with high computing performance up, and modulating the frequency of the core 80 with low computing performance down, thereby fully playing the computing performance of each core 80.

[0209] The chip frequency modulation apparatus 100 at least comprises a frequency setting module 10, a computational performance analysis module 20 and a frequency modulation module 30.

[0210] The frequency setting module 10 sets a plurality of working frequencies for the operational chip of the computing device, and causes the plurality of cores 80 in the operational chip to work at the respective working frequencies, wherein frequencies at each working frequency are different.

[0211] That is, the plurality of different working frequencies are set for each operational chip, and the respective cores 80 of the operational chip are caused to work at the respective working frequencies according to the frequency modulation mechanism of the operational chip. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. The number of working frequencies and a distance between the frequencies in the invention can be set according to actual needs, and the more the working frequencies are, the most likely the computing performance of the respective cores 80 will be fully played. When a frequency modulation switch is turned on (without modulating the frequencies of the cores 80), the cores 80 can be evenly distributed, unevenly distributed or randomly distributed to work at the working frequencies depending on a predetermined rule. Preferably, the frequency setting module 10 can set the plurality of working frequencies for the operational chip through a plurality of phase locked loops 70 shown in FIG. 2. Of course, the frequency setting module 10 also can set the plurality of working frequencies for the operational chip through other hardware or software.

[0212] The computational performance analysis module 20 analyzes a computing performance indicator of each core 80 at its current working frequency. The computing performance indicator represents the actual computing performance of the core 80 at the current working frequency, and includes, but is not limited to a computing correct ratio, a computing correct number, a computing speed and the like. If the computing performance indicator of the core 80 is high, it means that the computing performance of the core 80 may have room for improvement, and if the computing performance indicator of the core 80 is

low, it means that the computing performance of the core 80 may be insufficient to work at the frequency corresponding to the current working frequency.

[0213] The frequency modulation module 30 modulates the current working frequency of the core 80 up or down according to the computing performance indicator of the core 80 at the current working frequency. That is, according to the frequency modulation mechanism on a level of the cores, the core 80 is modulated to the suitable working frequency according to the actual computing performance of the core 80, the frequency of the core 80 with high computing performance is modulated up, and the frequency of the core 80 with low computing performance is modulated down, thereby fully playing the computing performance of each core 80. Preferably, the frequency of the core 80 is modulated periodically, if the computing correct ratio of the core 80 within the modulation period of the frequency reaches a first correct ratio threshold, it shows that the core 80 does not reach the best computing performance, so the current working frequency of the core 80 is modulated up to the higher upper working frequency, and if the computing correct ratio of the core 80 within the modulation period of the frequency does not reach a second correct ratio threshold, it shows that the computing performance of the core 80 is insufficient to work at the current working frequency, so the current working frequency of the core 80 is modulated down to the lower working frequency.

[0214] The chip frequency modulation apparatus 100 of the invention can be provided inside or outside the operational chip. The invention evaluates the working frequency of the core 80, modulates the corresponding frequency of the core 80, fully plays computing advantages of the core 80 with good performance, avoids the core with poor performance from influencing on the operating performance of the operational chip, and maximizes the computing performance of the respective cores 80 according to the actual computing performance of the respective cores 80 in the operational chip, thereby

improving the computing speed and the computing correct ratio of the operational chip and the overall computing device. Moreover, the core 80 of the operational chip in the invention does not jump among different frequencies, and the working frequency is relatively stable.

[0215] FIG. 2 is a structural diagram of a chip frequency modulation apparatus of a computing device in a first embodiment of the invention. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. Preferably, the computing device comprises a control board, and a hash board connected to the control board, the hash board is provided with at least one operational chip, and the operational chip is provided with a plurality of cores 80. Of course, the computing device also can comprise a radiator, a connection plate, a power module, and the like. The chip frequency modulation apparatus 100 at least comprises a frequency setting module 10, a computational performance analysis module 20 and a frequency modulation module 30.

[0216] The frequency setting module 10 sets a plurality of working frequencies for the operational chip through a plurality of phase locked loops 70, and causes the plurality of cores 80 in the operational chip to work at the respective working frequencies, wherein frequencies at the respective working frequencies are different, and the working frequencies and the phase locked loops 70 are in a one-to-one correspondence relationship. Preferably, the phase locked loops 70 are provided inside or outside the operational chip. The number of the respective working frequencies and a distance between the frequencies in the invention can be set according to actual needs, and the more the working frequencies are, the most likely the computing performance of the respective cores 80 will be fully played. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. Therefore, the invention can set more phase locked loops 70 to provide more working frequencies, thereby fully playing the computing performance of the respective cores 80.

[0217] It shall be noticed that a frequency difference between the working frequencies in the invention shall be controlled within a reasonable range, because when the core 80 is improved by one working frequency, the working frequency of the core is improved by one frequency difference, thereby improving certain computing performance due to improvement of the computing speed. Meanwhile, improvement of the working frequency of the core may cause loss of certain computing performance due to reduction of the computing correct ratio. Therefore, the frequency setting module 10 shall reasonably control the frequency difference between the adjacent working frequencies, such that when the core 80 is modulated up from the current working frequency to the upper working frequency, benefit of the computing performance of the core 80 shall be greater than loss. Preferably, a frequency difference between the adjacent working frequencies is from 1% to 10%.

[0218] The computational performance analysis module 20 analyzes a computing performance indicator of each core 80 at its current working frequency. The computing performance indicator represents the actual computing performance of the core 80 at the current working frequency, and includes, but is not limited to a computing correct ratio, a computing correct number, a computing speed and the like. If the computing performance indicator of the core 80 is high, it means that the computing performance of the core 80 may have room for improvement, and if the computing performance indicator of the core 80 is low, it means that the computing performance of the core 80 may be insufficient to work at the frequency corresponding to the current working frequency. Preferably, the computational performance analysis module 20 analyzes whether the computing performance indicator of the core 80 reaches predetermined first, second and/or third indicator thresholds in a predetermined modulation period, wherein the first indicator threshold is the same as or different from the second indicator threshold.

[0219] The frequency modulation module 30 modulates the current working frequency of the core 80 up or down through the phase locked loops 70 according to the computing performance indicator of the core 80. Of course, the frequency modulation module 30 also can modulate the current working frequency of the core 80 up or down through other hardware or software. Preferably, if the computing performance indicator of the core 80 reaches the first indicator threshold, the frequency modulation module 30 modulates the current working frequency of the core 80 up to the upper working frequency; and/or, if the computing performance indicator of the core 80 does not reach the second indicator threshold, the frequency modulation module 30 modulates the current working frequency of the core 80 down to the lower working frequency; and/or if the computing performance indicator of the core 80 reaches the third indicator threshold, the frequency modulation module 30 modulates the current working frequency of the core 80 down to the lower working frequency.

[0220] For example, taking “for example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set”, and the current working frequency of the core 80 to be 600 MHz for example, the computing performance indicator is the computing correct ratio of the core 80 within the modulation period, and the first indicator threshold and the second indicator threshold are both 90%. If the computing correct ratio of the core 80 within the modulation period reaches 90%, it means that the computing performance of the core 80 is good, so the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 650 MHz. If the computing correct ratio of the core 80 within the modulation period does not reach 90%, it means that the computing performance of the core 80 is poor, so the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 550 MHz. Those skilled in the art can understand that the upper working frequency is not limited to the upper

adjacent working frequency, and one or more upper adjacent working frequencies also can be the upper working frequency; the lower working frequency is not limited to the lower adjacent working frequency, and one or more lower adjacent working frequencies also can be the lower working frequency. That is, the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 700 MHz, the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 500 MHz, and so on. Here, a spacing between the upper working frequency and the lower working frequency is not limited. Preferably, a frequency difference between the current working frequency and the upper working frequency is from 1% to 10%, and a frequency difference between the current working frequency and the lower working frequency is from 1% to 10%, such that the core 80 is modulated up from the current working frequency to the upper working frequency or the lower working frequency, and benefit of the computing performance of the core 80 shall be greater than loss.

[0221] For another example, the computing performance indicator is the computing correct ratio of the core 80 within the modulation period, the first indicator threshold is 90%, and the second indicator threshold is 80%. If the computing correct ratio of the core 80 within the modulation period reaches 90%, it means that the computing performance of the core 80 is good, so the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 650 MHz. If the computing correct ratio of the core 80 within the modulation period does not reach 80%, it means that the computing performance of the core 80 is poor, so the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 550 MHz.

[0222] For still another example, the computing performance indicator is the number of correct computations and the number of wrong computations of the core 80 within the modulation period, the first indicator threshold is 100, and the second indicator

threshold is 10. If the number of correct computations of the core 80 within the modulation period reaches 100, it means that the computing performance of the core 80 is good, so the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 650 MHz. If the number of wrong computations of the core 80 within the modulation period reaches 10, it means that the computing performance of the core 80 is poor, so the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 550 MHz.

[0223] Preferably, the frequency modulation module 30 further comprises a frequency modulation sub-module 31 and a stop frequency modulation sub-module 32.

[0224] The frequency modulation sub-module modulates the current working frequency of the core 80 up or down according to the computing performance indicator of the core 80. Preferably, the frequency modulation sub-module 31 modulates the current working frequency of the core 80 up or down through phase locked loops 70 according to the computing performance indicator of the core 80. Of course, the frequency modulation sub-module 31 also can modulate the current working frequency of the core 80 up or down through other hardware or software.

[0225] The stop frequency modulation sub-module 32, if the cores 80 worked at the predetermined at least one optimized working frequency exceed a predetermined first ratio, stops modulating the frequencies of the cores 80; or if the number of cores 80 worked at the at least one optimized working frequency is maximum, stops modulating the frequencies of the cores 80.

[0226] For example, one or more optimized working frequencies can be selected and preset from the plurality of working frequencies, and if the working frequencies of most cores 80 have reached the optimized working frequencies, it shows that the working frequencies of the respective cores 80 in the operational chip have been in an optimized

state, thereby fully playing the computing performance of the respective cores 80 without further frequency modulation, so the working frequencies of the cores 80 are stopped modulation. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, two optimized working frequencies 600 MHz and 650 MHz are selected as optimized working frequencies, and if over 80% of the cores 80 are worked at the working frequencies 600 MHz and 650 MHz, the frequencies of the cores 80 are stopped modulation.

[0227] FIG. 3 is a structural diagram of a chip frequency modulation apparatus of a computing device in a second embodiment of the invention. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. Preferably, the computing device comprises a control board, and a hash board connected to the control board, the hash board is provided with at least one operational chip, and the operational chip is provided with a plurality of cores 80. Of course, the computing device also can comprise a radiator, a connection plate, a power module, and the like. The chip frequency modulation apparatus 100 at least comprises a frequency setting module 10, a computational performance analysis module 20 and a frequency modulation module 30.

[0228] The frequency setting module 10 sets a plurality of working frequencies for the operational chip of the computing device, and causes the plurality of cores 80 in the operational chip to work at the respective working frequencies, wherein frequencies at each working frequency are different. That is, according to the frequency modulation mechanism on a level of the operational chip, several different working frequencies are set for each operational chip, and the respective cores 80 of the operational chip are caused to work at the respective working frequencies. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. The number of working frequencies and a distance between the frequencies in the invention can be set according to

actual needs, and the more the working frequencies are, the most likely the computing performance of the respective cores 80 will be fully played. When a frequency modulation switch is turned on (without modulating the frequencies of the cores 80), the cores 80 can be evenly distributed, unevenly distributed or randomly distributed to work at the working frequencies depending on a predetermined rule. Preferably, the frequency setting module 10 sets the plurality of working frequencies for the operational chip through a plurality of phase locked loops 70 shown in FIG. 2, and causes the plurality of cores 80 in the operational chip to work at the respective working frequencies, and the working frequencies and the phase locked loops 70 are in a one-to-one correspondence relationship. Therefore, the invention can set more phase locked loops 70 to provide more working frequencies, thereby fully playing the computing performance of the respective cores 80. Of course, the frequency setting module 10 also can set the plurality of working frequencies for the operational chip through other hardware or software.

[0229] It shall be noticed that a frequency difference between the working frequencies in the invention shall be controlled within a reasonable range, because when the core 80 is improved by one working frequency, the working frequency of the core is improved by one frequency difference, thereby improving certain computing performance due to improvement of the computing speed. Meanwhile, improvement of the working frequency of the core may cause loss of certain computing performance due to reduction of the computing correct ratio. Therefore, the frequency setting module 10 shall reasonably control the frequency difference between the adjacent working frequencies, such that when the core 80 is modulated up from the current working frequency to the upper working frequency, benefit of the computing performance of the core 80 shall be greater than loss. Preferably, a frequency difference between the adjacent working frequencies is from 1% to 10%.

[0230] The computational performance analysis module 20 analyzes whether the computing correct ratio of the core 80 reaches predetermined first and/or second correct ratio thresholds in a predetermined modulation period, and the first correct ratio threshold is the same as or different from the second correct ratio threshold. If the computing correct ratio of the core 80 reaches the predetermined first correct ratio threshold, it means that the computing performance of the core 80 may have room for improvement. If the computing correct ratio of the core 80 does not reach the predetermined second correct ratio threshold, it means that the computing performance of the core 80 may be insufficient to work at the frequency corresponding to the current working frequency.

[0231] The frequency modulation module 30, if the computing correct ratio of the core 80 reaches the first correct ratio threshold, and shows that the core 80 does not reach the best computing performance, modulates the current working frequency of the core 80 up to the upper working frequency; and/or if the computing correct ratio of the core 80 does not reach the second correct ratio threshold, and shows that the computing performance of the core 80 is insufficient to work at the current working frequency, modulates the current working frequency of the core 80 down to the lower working frequency. The frequency modulation module 30 can modulate the frequency of the core 80 through the phase locked loops 70 shown in FIG. 2 or software. That is, according to the frequency modulation mechanism on a level of the cores, the core 80 is modulated to a suitable working frequency according to the actual computing performance of the core 80, the frequency of the core 80 with high computing performance is modulated up, and the frequency of the core 80 with low computing performance is modulated down, thereby fully playing the computing performance of each core 80.

[0232] For example, the first correct ratio threshold and the second correct ratio threshold are both 90%. When the core 80 is worked at 600 MHz, if the computing correct

ratio of the core 80 within the predetermined modulation period exceeds 90% (it shows that the core 80 does not reach the best computing performance), the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency, i.e., the working frequency is improved to 650 MHz. If the computing correct ratio of the core 80 is less than 90% (it shows that the computing performance of the core 80 is insufficient to work at the frequency of the current working frequency 600 MHz), the current working frequency of the core 80 is modulated down to the lower working frequency, i.e., the working frequency is reduced to 550 MHz. Those skilled in the art can understand that the upper working frequency is not limited to the upper adjacent working frequency, and one or more upper adjacent working frequencies also can be the upper working frequency; the lower working frequency is not limited to the lower adjacent working frequency, and one or more lower adjacent working frequencies also can be the lower working frequency. That is, the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 700 MHz, the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 500 MHz, and so on. Here, a spacing between the upper working frequency and the lower working frequency is not limited. Preferably, a frequency difference between the current working frequency and the upper working frequency is from 1% to 10%, and a frequency difference between the current working frequency and the lower working frequency is from 1% to 10%, such that the core 80 is modulated up from the current working frequency to the upper working frequency or the lower working frequency, and benefit of the computing performance of the core 80 shall be greater than loss.

[0233] For another example, the first correct ratio threshold is 90%, and the second correct ratio threshold is 80%. When the core 80 is worked at 600 MHz, if the computing correct ratio of the core 80 within the predetermined modulation period exceeds 90% (it shows that the core 80 does not reach the best computing performance), the current working

frequency of the core 80 is modulated up to the upper working frequency, i.e., the working frequency is improved to 650 MHz. If the computing correct ratio of the core 80 is less than 90% (it shows that the computing performance of the core 80 is insufficient to work at the frequency of the current working frequency 600 MHz), the current working frequency of the core 80 is modulated down to the lower working frequency, i.e., the working frequency is reduced to 550 MHz.

[0234] Preferably, the computing correct ratio can be a computing correct ratio of Nonces (Number once, random numbers) submitted by the cores 80 within the modulation period. That is, during a predetermined time, in all Nonces submitted by the cores 80, the computing correct ratio is a ratio occupied by correct Nonces. A block header in a blockchain comprises the Nonce (four bytes), Nonce is a random value, and the function of miners is actually to guess the value of Nonce, such that a hash of the block header can be less than a target value Target, and can be written into the blockchain. Specifically, this attribute starts from 0 to 2^{32} to compute the hash of the block header, and if the obtained hash result conforms to conditions, mining is successful.

[0235] Preferably, the computational performance analysis module 20 in FIG. 3 further comprises:

[0236] a first analysis sub-module 21 for analyzing whether the Nonces submitted by the core 80 are correct within the predetermined modulation period;

[0237] a counting sub-module 22 for counting the number of correct Nonces and the number of wrong Nonces submitted by the core 80 within the modulation period;

[0238] a first judgment module 23 for computing a computing correct ratio of Nonces of the core 80 within the modulation period according to the number of correct Nonces and the number of wrong Nonces, and judging whether the computing correct ratio of Nonces reaches the predetermined first and/or second correct ratio thresholds.

[0239] The frequency modulation module 30, if the computing correct ratio of Nonces of the core 80 reaches the first correct ratio threshold, modulates the current working frequency of the core 80 up to the upper working frequency; and/or if the computing correct ratio of Nonces of the core 80 does not reach the second correct ratio threshold, modulates the current working frequency of the core 80 down to the lower working frequency.

[0240] Most preferably, the first analysis sub-module 21 further comprises:

[0241] a first computing unit 211 for computing a first result from the Nonce through a predetermined algorithm every time when the core 80 submits one Nonce within the modulation period, the first result including a first feature, the first computing unit 211 preferably provided in the core 80. The Nonce submitted by each core 80 includes identification information (ID) of the Nonce, thereby counting the computing result of each core 80.

[0242] a first verification unit 212 for computing a second result from the Nonce submitted by the core 80 through the same algorithm, the second result including a second feature, if the first feature is the same as the second feature, judging that the Nonce is the correct Nonce, or the Nonce is the wrong Nonce. The first verification unit 212 is preferably provided in the operational chip.

[0243] For example, after the core 80 computes and submits one Nonce, the Nonce is embedded into the block header to compute a first hash result, and value of front twenty bits of the first hash result is 0 (the first feature). The first verification unit 212 also embeds the Nonce into the block header to compute a second hash result, and if value of front twenty bits of the second hash result is also 0 (the second feature), it is considered that the Nonce is one correct submission.

[0244] It shall be noted that in order to improve probability of the Nonce values satisfied for writing into the blockchain computed by the single core 80, the hash also can be judged using Target_Lite easier than the "target value Target", and each core can submit the Nonces more frequently. The first verification unit 212 verifies the Nonces submitted by the core 80, and if the hash computed by the Nonces submitted by the core 80 also passes judgment of the Target_Lite, it is considered that the core 80 submits correctly, or submits wrongly. The invention is not limited to use the Nonces capable of writing into the final blockchain. The interactive Nonce between the first verification unit 212 and the core 80 satisfies a lower threshold, has a higher submission density, and facilitates frequency modulation.

[0245] Preferably, the computational performance analysis module 20 real-time analyzes whether the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold and/or the second correct ratio threshold according to a preset real-time modulating instruction, and the first correct ratio threshold is the same as or different from the second correct ratio threshold.

[0246] If the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold, the frequency modulation module 30 real-time modulates the current working frequency of the core 80 up to the upper working frequency. If the computing correct ratio of the core 80 within the modulation period does not reach the second correct ratio threshold, the frequency modulation module 30 real-time modulates the current working frequency of the core 80 down to the lower working frequency, such that the working frequency of the core 80 is real-time modulated dynamically.

[0247] Preferably, the computational performance analysis module 20 analyzes whether the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold and/or the second correct ratio threshold according to a preset

timed modulating instruction within a modulation time period set by the timed modulating instruction, and the first correct ratio threshold is the same as or different from the second correct ratio threshold.

[0248] If the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold in the modulation time period, the frequency modulation module 30 modulates the current working frequency of the core 80 up to the upper working frequency. If the computing correct ratio of the core 80 within the modulation period does not reach the second correct ratio threshold in the modulation time period, the frequency modulation module 30 modulates the current working frequency of the core 80 down to the lower working frequency, such that the working frequency of the core 80 is timed modulated. If only Saturday (24 hours) per week is set to count the computing correct ratio of the core 80, frequency is modulated according to the computing correct ratio.

[0249] Preferably, the computational performance analysis module 20 analyzes whether the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold and/or the second correct ratio threshold according to a received immediate modulating instruction, and the first correct ratio threshold is the same as or different from the second correct ratio threshold.

[0250] According to the received immediate modulating instruction, if the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold, the frequency modulation module 30 modulates the current working frequency of the core 80 up to the upper working frequency, and if the computing correct ratio of the core 80 within the modulation period does not reach the second correct ratio threshold, the frequency modulation module 30 modulates the current working frequency of the core 80 down to the lower working frequency. According to a received stop modulating

instruction, the frequency modulation module 30 stops modulating the current working frequency of the core 80.

[0251] For example, users can timely send the immediate modulating instruction to the computing device according to needs, and the computing device immediately starts analyzing the computing correct ratio of the cores 80 according to the immediate modulating instruction. If the computing correct ratio of the cores 80 exceeds the first correct ratio threshold (e.g., over 99%) within the modulation period (e.g., 10 minutes), the working frequency of the cores 80 is modulated up, and if the computing correct ratio of the cores 80 is less than the second correct ratio threshold (e.g., below 99%) within the modulation period (e.g., 10 minutes), the working frequency of the cores 80 is modulated down. In addition, users can timely send stop modulating instruction to the computing device according to needs, and after receiving the stop modulating instruction, the computing device immediately stops modulating the frequency of the core 80.

[0252] FIG. 4 is a structural diagram of a chip frequency modulation apparatus of a computing device in a third embodiment of the invention. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. Preferably, the computing device comprises a control board, and a hash board connected to the control board, the hash board is provided with at least one operational chip, and the operational chip is provided with a plurality of cores 80. Of course, the computing device also can comprise a radiator, a connection plate, a power module, and the like. The chip frequency modulation apparatus 100 comprises a frequency setting module 10, a computational performance analysis module 20 and a frequency modulation module 30.

[0253] The frequency setting module 10 sets a plurality of working frequencies for the operational chip of the computing device, and causes the plurality of cores 80 in the operational chip to work at the respective working frequencies, wherein frequencies at each

working frequency are different. That is, according to the frequency modulation mechanism of the operational chip, the plurality of different working frequencies are set for each operational chip, and the respective cores 80 of the operational chip are caused to work at the respective working frequencies. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. The number of working frequencies and a distance between the frequencies in the invention can be set according to actual needs, and the more the working frequencies are, the most likely the computing performance of the respective cores 80 will be fully played. When a frequency modulation switch is turned on (without modulating the frequencies of the cores 80), the cores 80 can be evenly distributed, unevenly distributed or randomly distributed to work at the working frequencies depending on a predetermined rule. Preferably, the frequency setting module 10 can set the plurality of working frequencies for the operational chip through a plurality of phase locked loops 70 shown in FIG. 2. Of course, the frequency setting module 10 also can set the plurality of working frequencies for the operational chip through other hardware or software.

[0254] It shall be noticed that a frequency difference between the working frequencies in the invention shall be controlled within a reasonable range, because when the core 80 is improved by one working frequency, the working frequency of the core is improved by one frequency difference, thereby improving certain computing performance due to improvement of the computing speed. Meanwhile, improvement of the working frequency of the core may cause loss of certain computing performance due to reduction of the computing correct ratio. Therefore, the frequency setting module 10 shall reasonably control the frequency difference between the adjacent working frequencies, such that when the core 80 is modulated up from the current working frequency to the upper working frequency, benefit of the computing performance of the core 80 shall be greater than loss.

Preferably, a frequency difference between the adjacent working frequencies is from 1% to 10%.

[0255] The computational performance analysis module 20 analyzes a computing performance indicator of each core 80 at its current working frequency. The computational performance analysis module 20 further comprises:

[0256] a setting sub-module 24 for presetting a reference node value, a computing correct weight value, a computing wrong weight value, a computing correct threshold and a computing wrong threshold of the core 80. The computing correct weight value can be the same as or different from the computing wrong weight value, and the computing correct threshold can be the same as or different from the computing wrong threshold. The reference node value, the computing correct weight value, the computing wrong weight value, the computing correct threshold and the computing wrong threshold are all adjustable parameters, and can be optimized according to actual needs such as frequency modulation speed.

[0257] a second analysis sub-module 25 for analyzing whether each computation of the core 80 is correct. The core 80 can make various different computations to analyze whether each or few computations of the core 80 are correct. Preferably, whether the Nonces computed by the cores 80 are correct is analyzed.

[0258] a counting sub-module 26 for adding one computing correct weight value to the reference node value every time when the core 80 computes correctly at least once, and reducing one computing wrong weight value from the reference node value every time when the core 80 computes wrongly at least once. Preferably, one computing correct weight value is added to the reference node value every time when the core 80 computes correctly once. Of course, it can be set that one computing correct weight value is added to the reference node value every time when the core 80 computes correctly N (N is a natural

number greater than 1) times. One computing wrong weight value is reduced from the reference node value every time when the core 80 computes wrongly once. Of course, it can be set that one computing wrong weight value is reduced from the reference node value every time when the core 80 computes wrongly N (N is a natural number greater than 1) times.

[0259] a second judgment sub-module 27 for judging whether the current reference node value of the core 80 reaches the computing correct threshold or the computing wrong threshold. If the current reference node value reaches the computing correct threshold, it means that the computing performance of the core 80 is high, and may have room for improvement. If the current reference node value reaches the computing wrong threshold, it means that the computing performance of the core 80 is poor, and may be insufficient to work at the frequency corresponding to the current working frequency.

[0260] The frequency modulation module 30, if the current reference node value of the core 80 reaches the computing correct threshold, and shows that the core 80 does not reach the best computing performance, modulates the current working frequency of the core 80 up to the upper working frequency; and if the current reference node value of the core 80 reaches the computing wrong threshold, and shows that the computing performance of the core 80 is insufficient to work at its current working frequency, modulates the current working frequency of the core 80 down to the lower working frequency. The frequency modulation module 30 can modulate the frequency of the core 80 through the phase locked loops 70 shown in FIG. 2 or software. That is, according to the frequency modulation mechanism on a level of the cores, the core 80 is modulated to the suitable working frequency according to the actual computing performance of the core 80, the frequency of the core 80 with high computing performance is modulated up, and the frequency of the core 80 with low computing performance is modulated down, thereby fully playing the

computing performance of each core 80. Those skilled in the art can understand that the upper working frequency is not limited to the upper adjacent working frequency, and one or more upper adjacent working frequencies also can be the upper working frequency; the lower working frequency is not limited to the lower adjacent working frequency, and one or more lower adjacent working frequencies also can be the lower working frequency. That is, the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 700 MHz, the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 500 MHz, and so on. Here, a spacing between the upper working frequency and the lower working frequency is not limited. Preferably, a frequency difference between the current working frequency and the upper working frequency is from 1% to 10%, and a frequency difference between the current working frequency and the lower working frequency is from 1% to 10%, such that the core 80 is modulated up from the current working frequency to the upper working frequency or the lower working frequency, and benefit of the computing performance of the core 80 shall be greater than loss.

[0261] For example, as shown in FIG. 5, the reference node value is set to be 400,000, the computing correct weight value is set to be 180, the computing wrong weight value is set to be 9,000, and the computing correct threshold and the computing wrong threshold are both set to be 100,000.

[0262] 180 (the computing correct weight value) is added to the reference node value every time when the core 80 computes correctly once, 9,000 (the computing wrong weight value) is reduced from the reference node value every time when the core 80 computes wrongly once, and taking the reference node value for reference, the upper frequency or the lower frequency is stepped upward or downward every time when 100,000 (the computing correct threshold and the computing wrong threshold) is added or reduced.

[0263] The current mechanism is similar with wrong or correct tug-of-war mechanism, and correct and wrong mechanisms may have different weights. The reference node value is set. One computing correct weight value is added every time when one correct result is received, one computing wrong weight value is reduced every time when one wrong result is received, and if reward or punishment exceeds a corresponding threshold, the frequency is modulated up or down. It can be understood that the system has a marker, the reference node value is an initial value of the marker, maker + 180 for correct submission, and maker – 9,000 for each wrong submission. After Nth (N is a natural number greater than or equal to 1) corrects and Mth (M is a natural number greater than or equal to 1) errors, the marker shall be at a position of 400000 + N * 180–M*9000, and if the marker exceeds one threshold, the frequency is modulated correspondingly (i.e., modulating up or down). Then, every time when the frequency is modulated to a new frequency, the value is initialized, i.e., the current reference node value is reset to an initial reference node value.

[0264] Preferably, the setting sub-module 24 sets and adjusts the reference node value, the computing correct weight value, the computing wrong weight value, the computing correct threshold and/or the computing wrong threshold of the core 80 according to actual requirements, the computing correct weight value is the same as or different from the computing wrong weight value, and the computing correct threshold is the same as or different from the computing wrong threshold.

[0265] Preferably, the setting sub-module 24 controls an expected tolerant resident error ratio S of the core 80 by controlling a ratio of the computing correct weight value to the computing wrong weight value. A computing formula of the resident error ratio S is: the resident error ratio S = the computing correct weight value divided by the computing correct weight value and the computing wrong weight value.

[0266] Preferably, the setting sub-module 24 controls a modulation period by controlling an absolute value of the computing correct weight value and the computing wrong weight value.

[0267] Preferably, the setting sub-module controls the modulation period by controlling an absolute value of the computing correct threshold and the computing wrong threshold.

[0268] Preferably, the correct computation can be that the core 80 correctly computes the Nonce.

[0269] The second analysis sub-module 25 analyzes whether the Nonce submitted every time by the core 80 is correct.

[0270] The counting sub-module 26 adds one computing correct weight value to the reference node value every time when the core 80 submits at least one correct Nonce, and reduces one computing wrong weight value from the reference node value every time when the core 80 submits at least one wrong Nonce. Preferably, one computing correct weight value is added to the reference node value every time when the core 80 submits one correct Nonce. Of course, it also can be set that one computing correct weight value is added to the reference node value every time when the core 80 submits Nth (N is a natural number greater than 1) correct Nonces. One computing wrong weight value is reduced from the reference node value every time when the core 80 submits one wrong Nonce. Of course, it also can be set that one computing wrong weight value is reduced from the reference node value every time when the core 80 submits Nth (N is a natural number greater than 1) wrong Nonces.

[0271] More preferably, the second analysis sub-module 25 further comprises:

[0272] a second computing unit 251 for computing, via the core 80, a first result from the Nonce through a predetermined algorithm after the core 80 submits one Nonce, the first result including a first feature;

[0273] a second verification unit 252 for computing a second result from the Nonce through the same algorithm, the second result including a second feature. If the first feature is the same as the second feature, it is judged that the Nonce is the correct Nonce, or the Nonce is the wrong Nonce.

[0274] For example, after the core 80 computes and submits one Nonce, the Nonce is embedded into the block header to compute a first hash result, and value of front twenty bits of the first hash result is 0 (the first feature). The second verification unit 252 also embeds the Nonce into the block header to compute a second hash result, and if value of front twenty bits of the second hash result is also 0 (the second feature), it is considered that the Nonce is one correct submission.

[0275] It shall be noted that in order to improve probability of the Nonce values satisfied for writing into the blockchain computed by the single core 80, the hash also can be judged using Target_Lite easier than the “target value Target”, and each core can submit the Nonces more frequently. The first verification unit 212 verifies the Nonces submitted by the core 80, and if the hash computed by the Nonces submitted by the core 80 also passes judgment of the Target_Lite, it is considered that the core 80 submits correctly, or submits wrongly. The invention is not limited to use the Nonces capable of writing into the final blockchain. The interactive Nonce between the first verification unit 212 and the core 80 satisfies a lower threshold, has a higher submission density, and facilitates frequency modulation.

[0276] In one specific application embodiment of the invention, six phase locked loops 70 are used, and six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz,

700 MHz and 750 MHz are set. As shown in FIG. 5, the reference node value is set to be 400,000, the computing correct weight value is set to be 180, the computing wrong weight value is set to be 9,000, and the computing correct threshold and the computing wrong threshold are both set to be 100,000.

[0277] The number of cores distributed at the respective corresponding frequencies as counted by four hash boards is as follows:

[0278] Hash board 0: [294 26 96 224 1023 1665]

[0279] Hash board 1: [274 47 111 212 963 1721]

[0280] Hash board 2: [350 25 153 369 1381 1050]

[0281] Hash board 3: [488 33 184 367 1342 950]

[0282] Firstly, the mechanism is further explained with reference to data. According to the resident error ratio S = the computing correct weight value divided by the computing correct weight value and the computing wrong weight value, the resident error ratio S (which is understood to long-term reside on one frequency) of the core 80 can be inferred to be 180/（180+9000）=1.29% through the given data. Accordingly, the core 80 is worked at one frequency for a long time (because a desired step is 0), and the working frequency is not modulated up or down. It can be inferred that if a computing error ratio of the core 80 is greater than 1.29% (the resident error ratio S), the working frequency is modulated up, and if a computing error ratio of the core 80 is less than 1.29% (the resident error ratio S), the working frequency is modulated down.

[0283] According to difficulty of settings (the difficulty is associated with a verification reference, and has influence on the computing correct ratio of the core 80, and the larger a coefficient of difficulty is, the lower the correct ratio will be; in contrast, the higher the correct ratio will be), a substantial period of modulation when error rises can be inferred. Assuming that an error ratio is e, the desired step of each Nonce is: (1-e)*180-

e*9000=180-9180e. Taking e=0.5% for example, the desired step equals to 134.1, taking e=1% for example, the desired step equals to 88.2, and taking e=2% for example, the desired step equals to -3.6.

[0284] Computation is made using 650MHz, and an expectation of the single Nonce submitted by the core 80 is 1.3 per second (i.e., 1.3 Nonce is submitted within one second). Explanations are made using a scene where e is 0.5%, i.e., after 746 Nonces are submitted, the expectation can be modulated up once. When e is 1.0%, 1134 Nonces are submitted, and the expectation is modulated up once; if the error ratio is 2.0%, 27,778 Nonces are submitted, the expectation is modulated down once, and so on.

[0285] Preferably, the computational performance analysis module 20 real-time judges whether the current reference node value of the core 80 reaches the computing correct threshold or the computing wrong threshold according to a preset real-time modulating instruction, and the computing correct threshold is the same as or different from the computing wrong threshold.

[0286] The frequency modulation module 30, if the current reference node value of the core 80 reaches the computing correct threshold, real-time modulates the current working frequency of the core 80 up to the upper working frequency; if the current reference node value of the core 80 reaches the computing wrong threshold, real-time modulates the current working frequency of the core 80 down to the lower working frequency, such that the working frequency of the core 80 is real-time modulated dynamically.

[0287] Preferably, the computational performance analysis module 20 judges whether the current reference node value of the core 80 reaches the computing correct threshold or the computing wrong threshold according to a preset timed modulating instruction within a modulation time period set by the timed modulating instruction.

[0288] The frequency modulation module 30, if the current reference node value of the core 80 reaches the computing correct threshold in the modulation time period, modulates the current working frequency of the core 80 up to the upper working frequency; if the current reference node value of the core 80 reaches the computing wrong threshold in the modulation time period, modulates the current working frequency of the core 80 down to the lower working frequency, such that the working frequency of the core 80 is timed modulated. If only Saturday (24 hours) per week is set to count the number of the correct Nonces of the cores 80, the frequency is modulated according to the computing correct ratio.

[0289] Preferably, the computational performance analysis module 20 analyzes whether the current reference node value of the core 80 reaches the computing correct threshold or the computing wrong threshold according to a received immediate modulating instruction, and the computing correct threshold is the same as or different from the computing wrong threshold.

[0290] The frequency modulation module 30, according to the received immediate modulating instruction, if the current reference node value of the core 80 reaches the computing correct threshold, modulates the current working frequency of the core 80 up to the upper working frequency; if the current reference node value of the core 80 reaches the computing wrong threshold, modulates the current working frequency of the core 80 down to the lower working frequency. According to a received stop modulating instruction, the frequency modulation module 30 stops modulating the current working frequency of the core 80.

[0291] For example, users can timely send the immediate modulating instruction to the computing device according to needs, and users add a weight A to the reference node every time when the core 80 computes the correct Nonce once, and reduce a weight B from the reference node every time when the core 80 computes the wrong Nonce once. When the

currently added value reaches the computing correct number threshold C, the core 80 steps upward to the upper frequency. When the currently reduced value reaches the computing wrong number threshold D, the core 80 steps downward to the lower frequency. In addition, users can timely send stop modulating instruction to the computing device according to needs, and after receiving the stop modulating instruction, the computing device immediately stops modulating the frequency of the core 80.

[0292] FIG. 6 is a structural diagram of a chip frequency modulation apparatus of a computing device in a fourth embodiment of the invention. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. Preferably, the computing device comprises a control board, and a hash board connected to the control board, the hash board is provided with at least one operational chip, and the operational chip is provided with a plurality of cores 80. Of course, the computing device also can comprise a radiator, a connection plate, a power module, and the like. The chip frequency modulation apparatus 100 comprises a frequency setting module 10, a computational performance analysis module 20, a frequency modulation module 30, a frequency counting module 50 and a frequency modulation module 60.

[0293] The frequency setting module 10 sets a plurality of working frequencies for the operational chip of the computing device, and causes the plurality of cores 80 in the operational chip to work at the respective working frequencies. That is, according to the frequency modulation mechanism on a level of the operational chip, the plurality of different working frequencies are set for each operational chip, and the cores 80 of the operational chip are caused to work at the respective working frequencies. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. The number of working frequencies and a distance between the frequencies in the invention can be set according to actual needs, and the more the working frequencies are,

the most likely the computing performance of the respective cores 80 will be fully played. When a frequency modulation switch is turned on (without modulating the frequencies of the cores 80), the cores 80 can be evenly distributed, unevenly distributed or randomly distributed to work at the working frequencies depending on a predetermined rule. Preferably, the frequency setting module 10 can set the plurality of working frequencies for the operational chip through a plurality of phase locked loops (PPLs) 70 shown in FIG. 2. Of course, the frequency setting module 10 also can set the plurality of working frequencies for the operational chip through other hardware or software.

[0294] It shall be noticed that a frequency difference between the working frequencies in the invention shall be controlled within a reasonable range, because when the core 80 is improved by one working frequency, the working frequency of the core is improved by one frequency difference, thereby improving certain computing performance due to improvement of the computing speed. Meanwhile, improvement of the working frequency of the core may cause loss of certain computing performance due to reduction of the computing correct ratio. Therefore, the frequency setting module 10 shall reasonably control the frequency difference between the adjacent working frequencies, such that when the core 80 is modulated up from the current working frequency to the upper working frequency, benefit of the computing performance of the core 80 shall be greater than loss. Preferably, a frequency difference between the adjacent working frequencies is from 1% to 10%.

[0295] The computational performance analysis module 20 analyzes a computing performance indicator of each core 80 at its current working frequency. The computing performance indicator represents the actual computing performance of the core 80 at the current working frequency, and includes, but is not limited to a computing correct ratio, a computing correct number, a computing speed and the like. If the computing performance

indicator of the core 80 is high, it means that the computing performance of the core 80 may have room for improvement, and if the computing performance indicator of the core 80 is low, it means that the computing performance of the core 80 may be insufficient to work at the frequency corresponding to the current working frequency.

[0296] The frequency modulation module 30 modulates the current working frequency of the core 80 up or down according to the computing performance indicator of the core 80. That is, according to the frequency modulation mechanism on a level of the cores, the core 80 is modulated to the suitable working frequency according to the computing performance of the core 80, the frequency of the core 80 with high computing performance is modulated up, and the frequency of the core 80 with low computing performance is modulated down, thereby fully playing the computing performance of each core 80. The frequency modulation module 30 can modulate the frequency of the core 80 through the phase locked loops 70 shown in FIG. 2 or software. Preferably, if the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold, it shows that the core 80 does not reach the best computing performance, so the current working frequency of the core 80 is modulated up to the upper working frequency. If the computing correct ratio of the core 80 within the modulation period reaches the second correct ratio threshold, it shows that the computing performance of the core 80 is insufficient to work at the current working frequency, so the current working frequency of the core 80 is modulated down to the lower working frequency. Those skilled in the art can understand that the upper working frequency is not limited to the upper adjacent working frequency, and one or more upper adjacent working frequencies also can be the upper working frequency; the lower working frequency is not limited to the lower adjacent working frequency, and one or more lower adjacent working frequencies also can be the lower working frequency. That is, the current working frequency 600 MHz of the core 80 is

modulated up to the upper working frequency 700 MHz, the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 500 MHz, and so on. Here, a spacing between the upper working frequency and the lower working frequency is not limited. Preferably, a frequency difference between the current working frequency and the upper working frequency is from 1% to 10%, and a frequency difference between the current working frequency and the lower working frequency is from 1% to 10%, such that the core 80 is modulated up from the current working frequency to the upper working frequency or the lower working frequency, and benefit of the computing performance of the core 80 shall be greater than loss.

[0297] The frequency counting module 50 counts current distribution state of the cores 80 after frequency modulation at the respective working frequencies. After the working frequency is automatically modulated according to the computing performance itself, the cores 80 are distributed to work at the respective working frequencies, and the frequency counting module 50 counts the distributed number of the cores 80 after frequency modulation at the respective working frequencies, and can obtain the current distribution state. Preferably, the working frequency can be divided to comprise at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, and the minimum frequency in the low-frequency working frequency is a minimum working frequency. For example, there are totally one thousand cores 80, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, and the number of cores 80 sequentially distributed at the six working frequencies is 100, 200, 100, 100, 200 and 300, respectively. 500 MHz and 550 MHz are low-frequency working frequencies, 600 MHz and 650 MHz are middle working frequencies, and 700 MHz and 750 MHz are high-frequency working frequency.

500 MHz is the minimum working frequency, and 750 MHz is the maximum working frequency.

[0298] The frequency modulation module 60 modulates a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism of the cores 80. The frequency modulation mechanism is a correspondence relationship between the distribution state and the frequency modulation of the cores. The distribution state of the cores refers to a distribution state of the cores 80 worked at the respective working frequencies. Modulating a frequency in the working frequency refers to directly modulate the frequency in the working frequency. Preferably, the frequency modulation module 60 modulates the frequency in the working frequency through the phase locked loops 70 shown in FIG. 2. Those skilled in the art can understand that the modulation way of the frequency counting module 50 modulating the working frequency is not limited thereto. An ideal state of the invention is to hope that over a predetermined ratio (e.g., 50%) or the maximum number of cores 80 falls into the middle working frequencies, such that the frequencies of the cores 80 have a large room for modulation up.

[0299] For example, if over a predetermined ratio (e.g., 30%) of cores 80 are worked at the high working frequency (750 MHz), it may cause that the cores 80 do not play the maximum computing performance (which may be higher), so one working frequency (600 MHz) is modified to at least one optimized high-frequency working frequency (800 MHz), and the cores 80 originally worked at the working frequency (600 MHz) are all transferred to work at the maximum working frequency (750 MHz). The frequency in the optimized high-frequency working frequency is higher than the frequency in the maximum working frequency, thereby fully playing the computing performance of the respective cores 80.

[0300] In one specific embodiment of the invention, the frequency modulation module 60 further comprises a first frequency modulation sub-module 61 and/or a second frequency modulation sub-module 62.

[0301] If the cores 80 exceeding a predetermined second ratio are worked at the at least one high-frequency working frequency, and may cause that the cores 80 do not play the maximum computing performance (which may be higher), the first frequency modulation sub-module 61 modifies the at least one working frequency to at least one optimized high-frequency working frequency, and a frequency in the optimized high-frequency working frequency is higher than a frequency in the maximum working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0302] For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, and if over 30% (the second ratio) of the cores 80 are worked at the two high-frequency working frequencies (700 MHz and 750 MHz), the two low-frequency working frequencies (500 MHz and 550 MHz) are modified to two optimized high-frequency working frequencies (800 MHz and 850 MHz), or one low-frequency working frequency (500 MHz) and one middle working frequency (600 MHz) are modified to two optimized high-frequency working frequencies (800 MHz and 850 MHz).

[0303] Preferably, if the cores 80 exceeding the second ratio are worked at the maximum working frequency, and may cause that the cores 80 do not play the maximum computing performance (which may be higher), the first frequency modulation sub-module 61 modifies the one working frequency to the one optimized high-frequency working frequency, and a frequency in the optimized high-frequency working frequency is higher than a frequency in the maximum working frequency. The modified working frequency can

be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0304] For example, if over 30% (the second ratio) of the cores 80 are worked at the maximum working frequency (750 MHz), one low-frequency working frequency (500 MHz) is modified to an optimized high-frequency working frequency (800 MHz), or one middle working frequency (600 MHz) is modified to an optimized high-frequency working frequency (800 MHz), or the maximum working frequency (750 MHz) is modified to an optimized high-frequency working frequency (800 MHz).

[0305] If the cores 80 exceeding a predetermined third ratio are worked at the at least one low-frequency working frequency, and means that the computing capability of the cores 80 is too poor to be insufficient to work at the low-frequency working frequency, the second frequency modulation sub-module 62 modifies the at least one working frequency to at least one optimized low-frequency working frequency, and a frequency in the optimized low-frequency working frequency is lower than a frequency in the minimum working frequency, thereby avoiding the cores 80 with poor computing performance from influencing on overall computing performance of the operational chip. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0306] For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, and if over 30% (the third ratio) of the cores 80 are worked at the two low-frequency working frequencies (500 MHz and 550 MHz), the two low-frequency working frequencies (500 MHz and 550 MHz) are modified to two optimized low-frequency working frequencies (400 MHz and 450 MHz), or one low-frequency working frequency (500 MHz) and one middle working frequency (600 MHz) are modified to two optimized low-frequency working frequencies (400 MHz and 450 MHz).

[0307] Preferably, if the cores 80 exceeding the third ratio are worked at the minimum working frequency, and means that the computing capability of the cores 80 is too poor to be insufficient to work at the minimum working frequency, the second frequency modulation sub-module 62 modifies the one working frequency to the one optimized low-frequency working frequency, and a frequency in the optimized low-frequency working frequency is lower than a frequency in the minimum working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0308] For example, if over 30% (the third ratio) of the cores 80 are worked at the minimum working frequency (500 MHz), one low-frequency working frequency (500 MHz) is modified to an optimized low-frequency working frequency (450 MHz), or one middle working frequency (600 MHz) is modified to an optimized low-frequency working frequency (450 MHz), or the maximum working frequency (750 MHz) is modified to an optimized low-frequency working frequency (450 MHz).

[0309] In one specific application embodiment of the invention, six phase locked loops 70 are used, and six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set.

[0310] The number of cores distributed at the respective corresponding frequencies as counted by four hash boards is as follows:

[0311] Hash board 0: [294 26 96 224 1023 1665]

[0312] Hash board 1: [274 47 111 212 963 1721]

[0313] Hash board 2: [350 25 153 369 1381 1050]

[0314] Hash board 3: [488 33 184 367 1342 950]

[0315] Taking the four hash boards 0-3 for example, as shown in FIG. 7, data substantially conform to a normal distribution, and the minimum working frequency (500

MHz) is the minimum frequency where the single core 80 is worked, and is unable to be modulated down (if the error ratio is too high, it can consider closing the minimum frequency). If over the predetermined ratio (e.g., 50%) of the cores 80 are accumulated at the maximum working frequency (750 MHz), it means not playing the maximum efficiency (which may be higher), and the entire operational chip has further room for improvement. A relative ideal state is that over the predetermined ratio (e.g., 50%) or the maximum number of cores 80 falls into one or more middle working frequencies, such as, the third working frequency (600 MHz). To fully use the computing performance of the cores 80, a long tail at the high performance side, rather than a long tail at the low frequency, shall be considered.

[0316] Taking the hash boards 0-1 for example, it can be seen that if the frequency 600 MHz is removed, and if left shift as a whole is used, generally, one hundred cores 80 fall at the frequency 550 MHz, and the current frequency is obviously in a left low-frequency region, which does not facilitate fully playing the computing performance of the cores 80. Therefore, right shift as a whole is more suitable, i.e., a whole shifting way. If the frequency 550 MHz is set to right as a whole to above the frequency 800 MHz through the phase locked loops 70 shown in FIG. 2, it is expected that several hundreds of the cores 80 are improved over 800 MHz, thereby improving the overall computing performance.

[0317] In another specific embodiment of the invention, the frequency modulation module 60 further comprises a third frequency modulation sub-module 63 and/or a fourth frequency modulation sub-module 64.

[0318] If the number of cores 80 worked at the at least one high-frequency working frequency is maximum, and may cause that the cores 80 do not play the maximum computing performance (which may be higher), the third frequency modulation sub-module 63 modifies the at least one working frequency to at least one optimized high-frequency working frequency, and a frequency in the optimized high-frequency working frequency is

higher than a frequency in the maximum working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0319] For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, and the maximum number of the cores 80 is worked at the two high-frequency working frequencies (700 MHz and 750 MHz), so the two low-frequency working frequencies (500 MHz and 550 MHz) are modified to two optimized high-frequency working frequencies (800 MHz and 850 MHz), or one low-frequency working frequency (500 MHz) and one middle working frequency (600 MHz) are modified to two optimized high-frequency working frequencies (800 MHz and 850 MHz).

[0320] Preferably, if the number of cores 80 worked at the maximum working frequency is maximum, and may cause that the cores 80 do not play the maximum computing performance (which may be higher), the third frequency modulation sub-module 63 modifies one working frequency to one optimized high-frequency working frequency, and a frequency in the optimized high-frequency working frequency is higher than a frequency in the maximum working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0321] For example, when the maximum number of the cores 80 are worked at the maximum working frequency (750 MHz), one low-frequency working frequency (500 MHz) is modified to an optimized high-frequency working frequency (800 MHz), or one middle working frequency (600 MHz) is modified to an optimized high-frequency working frequency (800 MHz), or the maximum working frequency (750 MHz) is modified to an optimized high-frequency working frequency (800 MHz).

[0322] If the number of cores 80 worked at the at least one low-frequency working frequency is maximum, and means that the computing capability of the cores 80 is too poor to be insufficient to work at the low-frequency working frequency, the fourth frequency modulation sub-module 64 modifies the at least one working frequency to at least one optimized low-frequency working frequency, and a frequency in the optimized low-frequency working frequency is lower than a frequency in the minimum working frequency, thereby avoiding the cores 80 with poor computing capability from influencing on the overall computing performance of the operational chip. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0323] For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, and the maximum number of the cores 80 is worked at the two low-frequency working frequencies (500 MHz and 550 MHz), so the two low-frequency working frequencies (500 MHz and 550 MHz) are modified to two optimized low-frequency working frequencies (400 MHz and 450 MHz), or one low-frequency working frequency (500 MHz) and one middle working frequency (600 MHz) are modified to two optimized low-frequency working frequencies (400 MHz and 450 MHz).

[0324] Preferably, if the number of cores 80 worked at the minimum working frequency is maximum, and means that the computing capability of the cores 80 is too poor to be insufficient to work at the minimum working frequency, the fourth frequency modulation sub-module 64 modifies one working frequency to one optimized low-frequency working frequency, and a frequency in the optimized low-frequency working frequency is lower than a frequency in the minimum working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0325] For example, when the maximum number of the cores 80 are worked at the minimum working frequency (500 MHz), one low-frequency working frequency (500 MHz) is modified to an optimized low-frequency working frequency (450 MHz), or one middle working frequency (600 MHz) is modified to an optimized low-frequency working frequency (450 MHz), or the maximum working frequency (750 MHz) is modified to an optimized low-frequency working frequency (450 MHz).

[0326] In one specific application embodiment of the invention, six phase locked loops 70 are used, and six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set.

[0327] The number of cores distributed at the respective corresponding frequencies as counted by four hash boards is as follows:

[0328] Hash board 0: [294 26 96 224 1023 1665]

[0329] Hash board 1: [274 47 111 212 963 1721]

[0330] Hash board 2: [350 25 153 369 1381 1050]

[0331] Hash board 3: [488 33 184 367 1342 950]

[0332] Taking the four hash boards 0-3 for example, as shown in FIG. 7, data substantially conforms to a normal distribution, and the minimum working frequency (500 MHz) is the minimum frequency where the single core 80 is worked, and is unable to be modulated down (if the error ratio is too high, it can consider closing the minimum frequency). If the number of cores 80 accumulated at the maximum working frequency (750 MHz) is maximum, it means not playing the maximum efficiency (which may be higher), and the entire operational chip has further room for improvement. A relative ideal state is that over the predetermined ratio (e.g., 50%) or the maximum number of cores 80 falls into one or more middle working frequencies, such as, the third working frequency (600 MHz).

To fully use the computing performance of the cores 80, a long tail at the high performance side, rather than a long tail at the low frequency, shall be considered.

[0333] Taking the hash boards 0-1 for example, it can be seen that if the frequency 600 MHz is removed, generally, one hundred cores 80 fall at the frequency 550 MHz, and the current frequency is obviously in a left low-frequency region. Therefore, right shift as a whole is more suitable, i.e., a whole shifting way. If the frequency 550 MHz is set to right as a whole to above the frequency 800 MHz through the phase locked loops 70 shown in FIG. 2, it is expected that several hundreds of the cores 80 are improved over 800 MHz, thereby improving the overall performance.

[0334] In still another specific embodiment of the invention, the frequency modulation module 60 further comprises a first stop modulation module 65 or a second stop modulation module 66.

[0335] If the cores 80 exceeding a predetermined fourth ratio are worked at the at least one middle working frequency, the first stop modulation module 65 stops modulating the frequency in the working frequency, because a relative ideal state is that over the predetermined fourth ratio (e.g., 50%) of the cores 80 falls into one or more middle working frequencies, such as, the third working frequency (600 MHz), which can fully play the working performance of the cores 80, so frequency modulation of the cores 80 is unnecessary.

[0336] If the number of cores 80 worked at the at least one middle working frequency is maximum, the second stop modulation module 66 stops modulating the frequency in the working frequency, because a relative ideal state is that the maximum number of the cores 80 falls into one or more middle working frequencies, such as, the third working frequency (600 MHz), which can fully play the working performance of the cores 80, so frequency modulation of the cores 80 is unnecessary.

[0337] The invention further provides a hash board comprising the chip frequency modulation apparatus 100.

[0338] The invention further provides a computing device comprising the chip frequency modulation apparatus 100.

[0339] FIG. 8 is a flow diagram of a chip frequency modulation method of a computing device according to the invention, which can be implemented by the chip frequency modulation apparatus 100 of the computing device. The computing device comprises at least one operational chip, and the operational chip is provided with a plurality of cores. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. It shall be noted that chip frequency modulation technique of the invention actually relates to two levels of frequency modulation mechanism, i.e., a frequency modulation mechanism on a level of the operational chip, and a frequency modulation mechanism on a level of the cores. The frequency modulation mechanism on a level of the operational chip refers to setting a plurality of suitable working frequencies for each operational chip, and causing the respective cores 80 of the operational chip to work at the respective working frequencies, thereby fully play working performance of each core 80. The frequency modulation mechanism on a level of the cores refers to modulating the core 80 to suitable working frequencies according to the actual computing performance of the core 80, modulating the frequency of the core 80 with high computing performance up, and modulating the frequency of the core 80 with low computing performance down, thereby playing the computing performance of each core 80. The method comprises steps of:

[0340] Step S801, setting a plurality of working frequencies for the operational chip of the computing device and causing the plurality of cores 80 in the operational chip to work at the respective working frequencies.

[0341] The step sets a plurality of working frequencies for each operational chip, and causes the respective cores 80 in the operational chip to work at the respective working frequencies according to the frequency modulation mechanism of the operational chip. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. The number of working frequencies and a distance between the frequencies in the invention can be set according to actual needs, and the more the working frequencies are, the most likely the computing performance of the respective cores 80 will be fully played. When a frequency modulation switch is turned on (without modulating the frequencies of the cores 80), the cores 80 can be evenly distributed, unevenly distributed or randomly distributed to work at the working frequencies depending on a predetermined rule. Preferably, the step can set a plurality of working frequencies for the operational chip through a plurality of phase locked loops 70 shown in FIG. 2. Of course, the method also can set a plurality of working frequencies for the operational chip through other hardware or software.

[0342] Step S802, analyzing a computing performance indicator of each core 80 at its current working frequency.

[0343] The computing performance indicator represents the actual computing performance of the core 80 at the current working frequency, and includes, but is not limited to a computing correct ratio, a computing correct number, a computing speed and the like. If the computing performance indicator of the core 80 is high, it means that the computing performance of the core 80 may have room for improvement, and if the computing performance indicator of the core 80 is low, it means that the computing performance of the core 80 may be insufficient to work at the frequency corresponding to the current working frequency.

[0344] Step S803, modulating the current working frequency of the core 80 up or down according to the computing performance indicator of the core 80.

[0345] According to the frequency modulation mechanism of the cores, the step modulates the core 80 to the suitable working frequency according to the actual computing performance of the core 80, modulates the frequency of the core 80 with high computing performance up, and modulates the frequency of the core 80 with low computing performance down, thereby fully playing the computing performance of each core 80. Preferably, if the computing correct ratio of the core 80 within the modulation period reaches a first correct ratio threshold, it shows that the core 80 does not reach the best computing performance, so the current working frequency of the core 80 is modulated up to the upper working frequency, and if the computing correct ratio of the core 80 within the modulation period does not reach a second correct ratio threshold, it shows that the computing performance of the core 80 is insufficient to work at the current working frequency, so the current working frequency of the core 80 is modulated down to the lower working frequency.

[0346] The invention evaluates the working frequency of the core 80, modulates the corresponding frequency of the core 80, fully plays computing advantages of the core 80 with good performance, avoids the core with poor performance from influencing on the operating performance of the operational chip, and maximized the computing performance of the respective cores 80 according to the actual computing performance of the respective cores 80 in the operational chip, thereby improving the computing speed and the computing correct ratio of the operational chip and the overall computing device. Moreover, the core 80 of the operational chip in the invention does not change among frequencies, and the working frequency is relatively stable.

[0347] FIG. 9 is a flow diagram of a chip frequency modulation method of a computing device in the first embodiment of the invention, which can be implemented by the chip frequency modulation apparatus 100 of the computing device shown in FIG. 2. The computing device comprises at least one operational chip, and the operational chip is provided with a plurality of cores. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. The method comprises steps of:

[0348] Step S901, setting the plurality of working frequencies for the operational chip through a plurality of phase locked loops 70, the working frequencies and the phase locked loops 70 being in a one-to-one correspondence relationship.

[0349] Preferably, the phase locked loops 70 shown in FIG. 2 are provided inside or outside the operational chip. The number of working frequencies and a distance between the frequencies in the invention can be set according to actual needs, and the more the working frequencies are, the most likely the computing performance of the respective cores 80 will be fully played. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. Therefore, the invention can set more phase locked loops 70 to provide more working frequencies, thereby fully playing the computing performance of the respective cores 80.

[0350] It shall be noticed that a frequency difference between the working frequencies in the invention shall be controlled within a reasonable range, because when the core 80 is improved by one working frequency, the working frequency of the core is improved by one frequency difference, thereby improving certain computing performance due to improvement of the computing speed. Meanwhile, improvement of the working frequency of the core may cause loss of certain computing performance due to reduction of the computing correct ratio. Therefore, the frequency setting module 10 shall reasonably control the frequency difference between the adjacent working frequencies, such that when

the core 80 is modulated up from the current working frequency to the upper working frequency, benefit of the computing performance of the core 80 shall be greater than loss. Preferably, a frequency difference between the adjacent working frequencies is from 1% to 10%.

[0351] Step S902, analyzing a computing performance indicator of each core 80 at its current working frequency.

[0352] The computing performance indicator represents the actual computing performance of the core 80 at the current working frequency, and includes, but is not limited to a computing correct ratio, a computing correct number, a computing speed and the like. If the computing performance indicator of the core 80 is high, it means that the computing performance of the core 80 may have room for improvement, and if the computing performance indicator of the core 80 is low, it means that the computing performance of the core 80 may be insufficient to work at the frequency corresponding to the current working frequency.

[0353] Preferably, the step analyzes whether the computing performance indicator of the core 80 reaches predetermined first, second and/or third indicator thresholds within a predetermined modulation period, the first indicator threshold being the same as or different from the second indicator threshold.

[0354] Step S903, modulating the current working frequency of the core 80 up or down through the phase locked loops 70 shown in FIG. 2 according to the computing performance indicator of the core 80. Of course, the step also can modulate the current working frequency of the core 80 up or down through other hardware or software.

[0355] Preferably, the step further comprises:

[0356] (1) if the computing performance indicator of the core 80 reaches the first indicator threshold, modulating the current working frequency of the core 80 up to the upper working frequency;

[0357] (2) if the computing performance indicator of the core 80 does not reach the second indicator threshold, modulating the current working frequency of the core 80 down to the lower working frequency; and/or

[0358] (3) if the computing performance indicator of the core 80 reaches the third indicator threshold, modulating the current working frequency of the core 80 down to the lower working frequency.

[0359] For example, taking "for example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set", and the current working frequency of the core 80 to be 600 MHz for example, the computing performance indicator is the computing correct ratio of the core 80 within the modulation period, and the first indicator threshold and the second indicator threshold are both 90%. If the computing correct ratio of the core 80 within the modulation period reaches 90%, it means that the computing performance of the core 80 is good, so the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 650 MHz. If the computing correct ratio of the core 80 within the modulation period does not reach 90%, it means that the computing performance of the core 80 is poor, so the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 550 MHz. Those skilled in the art can understand that the upper working frequency is not limited to the upper adjacent working frequency, and one or more upper adjacent working frequencies also can be the upper working frequency; the lower working frequency is not limited to the lower adjacent working frequency, and one or more lower adjacent working frequencies also can be the lower working frequency. Preferably, a frequency difference between the current

working frequency and the upper working frequency is from 1% to 10%, and a frequency difference between the current working frequency and the lower working frequency is from 1% to 10%, such that the core 80 is modulated up from the current working frequency to the upper working frequency or the lower working frequency, and benefit of the computing performance of the core 80 shall be greater than loss. That is, the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 700 MHz, the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 500 MHz, and so on. Here, a spacing between the upper working frequency and the lower working frequency is not limited.

[0360] For another example, the computing performance indicator is the computing correct ratio of the core 80 within the modulation period, the first indicator threshold is 90%, and the second indicator threshold is 80%. If the computing correct ratio of the core 80 within the modulation period reaches 90%, it means that the computing performance of the core 80 is good, so the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 650 MHz. If the computing correct ratio of the core 80 within the modulation period does not reach 80%, it means that the computing performance of the core 80 is poor, so the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 550 MHz.

[0361] For still another example, the computing performance indicator is the number of correct computations and the number of wrong computations of the core 80 within the modulation period, the first indicator threshold is 100, and the second indicator threshold is 10. If the number of correct computations of the core 80 within the modulation period reaches 100, it means that the computing performance of the core 80 is good, so the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 650 MHz. If the number of wrong computations of the core 80 within the

modulation period reaches 10, it means that the computing performance of the core 80 is poor, so the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 550 MHz.

[0362] Step S904, if the cores 80 worked at the predetermined at least one optimized working frequency exceed a predetermined first ratio, stopping modulating the frequencies of the cores 80; or if the number of cores 80 worked at the at least one optimized working frequency is maximum, stopping modulating the frequencies of the cores 80.

[0363] For example, one or more optimized working frequencies can be selected and preset from the plurality of working frequencies, and if the working frequencies of most cores 80 have reached the optimized working frequencies, it shows that the working frequencies of the respective cores 80 in the operational chip have been in an optimized state, thereby fully playing the computing performance of the respective cores 80 without further frequency modulation, so the working frequencies of the cores 80 are stopped modulation. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, two optimized working frequencies 600 MHz and 650 MHz are selected as optimized working frequencies, and if over 50% of the cores 80 are worked at the working frequencies 600 MHz and 650 MHz, the frequencies of the cores 80 are stopped modulation.

[0364] FIG. 10 is a flow diagram of a chip frequency modulation method of a computing device in the second embodiment of the invention, which can be implemented by the chip frequency modulation apparatus 100 of the computing device shown in FIG. 3. The computing device comprises at least one operational chip, and the operational chip is provided with a plurality of cores. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. The method comprises steps of:

[0365] Step S1001, setting a plurality of working frequencies for the operational chip of the computing device and causing the plurality of cores 80 in the operational chip to work at the respective working frequencies.

[0366] The step sets a plurality of working frequencies for each operational chip, and causes the plurality of cores 80 in the operational chip to work at the respective working frequencies according to the frequency modulation mechanism on a level of the operational chip. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. The number of working frequencies and a distance between the frequencies in the invention can be set according to actual needs, and the more the working frequencies are, the most likely the computing performance of the respective cores 80 will be fully played. When a frequency modulation switch is turned on (without modulating the frequencies of the cores 80), the cores 80 can be evenly distributed, unevenly distributed or randomly distributed to work at the working frequencies depending on a predetermined rule.

[0367] Preferably, the step sets the plurality of working frequencies for the operational chip through a plurality of phase locked loops 70 shown in FIG. 2, and causes the plurality of cores 80 in the operational chip to work at the respective working frequencies, and the working frequencies and the phase locked loops 70 are in a one-to-one correspondence relationship. The invention can set more phase locked loops 70 to provide more working frequencies, such that the computing performance of the respective cores 80 are fully played. Of course, the method also can set the plurality of working frequencies for the operational chip through other hardware or software.

[0368] It shall be noticed that a frequency difference between the working frequencies in the invention shall be controlled within a reasonable range, because when the core 80 is improved by one working frequency, the working frequency of the core is improved by one frequency difference, thereby improving certain computing performance

due to improvement of the computing speed. Meanwhile, improvement of the working frequency of the core may cause loss of certain computing performance due to reduction of the computing correct ratio. Therefore, a frequency difference between the adjacent working frequencies shall be reasonably controlled, such that when the core 80 is modulated up from the current working frequency to the upper working frequency, benefit of the computing performance of the core 80 shall be greater than loss. Preferably, a frequency difference between the adjacent working frequencies is from 1% to 10%.

[0369] Step S1002, analyzing whether a computing correct ratio of the core 80 reaches predetermined first and/or second correct ratio thresholds within a predetermined modulation period. The first correct ratio threshold is the same or different from the second correct ratio threshold. If the computing correct ratio of the core 80 reaches the predetermined first correct ratio threshold, it means that the computing performance of the core 80 may have room for improvement. If the computing correct ratio of the core 80 does not reach the predetermined second correct ratio threshold, it means that the computing performance of the core 80 may be insufficient to work at the frequency corresponding to the current working frequency.

[0370] Preferably, the step S1002 further comprises:

[0371] (1) real-time analyzing whether the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold and/or the second correct ratio threshold according to a preset real-time modulating instruction;

[0372] (2) analyzing whether the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold and/or the second correct ratio threshold according to a preset timed modulating instruction within a modulation time period set by the timed modulating instruction; or

[0373] (3) analyzing whether the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold and/or the second correct ratio threshold according to a received immediate modulating instruction.

[0374] Step S1003, if the computing correct ratio of the core 80 reaches the first correct ratio threshold, and shows that the core 80 does not reach the best computing performance, modulating the current working frequency of the core 80 up to the upper working frequency.

[0375] Preferably, the step further comprises:

[0376] (1) if the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold, real-time modulating the current working frequency of the core 80 up to the upper working frequency;

[0377] (2) if the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold in the modulation time period, modulating the current working frequency of the core 80 up to the upper working frequency; or

[0378] (3) according to the received immediate modulating instruction, if the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold, modulating the current working frequency of the core 80 up to the upper working frequency; according to a received stop modulating instruction, stopping modulating the current working frequency of the core 80.

[0379] For example, users can timely send the immediate modulating instruction to the computing device according to needs, and the computing device immediately starts analyzing the computing correct ratio of the core 80 according to the immediate modulating instruction. If the computing correct ratio of the core 80 exceeds the first correct ratio threshold (e.g., over 99%) within the modulation period (e.g., 10 minutes), the working frequency of the core 80 is modulated up, and if the computing correct ratio of the core 80

is less than the second correct ratio threshold (e.g., below 99%) within the modulation period (e.g., 10 minutes), the working frequency of the core 80 is modulated down. In addition, users can timely send stop modulating instruction to the computing device according to needs, and after receiving the stop modulating instruction, the computing device immediately stops modulating the frequency of the core 80.

[0380] Step S1004, if the computing correct ratio of the core 80 does not reach the second correct ratio threshold, and shows that the computing performance of the core 80 is insufficient to work at the current working frequency, modulating the current working frequency of the core 80 down to the lower working frequency.

[0381] Preferably, the step further comprises:

[0382] (1) if the computing correct ratio of the core 80 within the modulation period does not reach the second correct ratio threshold, real-time modulating the current working frequency of the core 80 down to the lower working frequency;

[0383] (2) if the computing correct ratio of the core 80 within the modulation period does not reach the second correct ratio threshold in the modulation time period, modulating the current working frequency of the core 80 down to the lower working frequency; or

[0384] (3) if the computing correct ratio of the core 80 within the modulation period does not reach the second correct ratio threshold, modulating the current working frequency of the core 80 down to the lower working frequency; according to a received stop modulating instruction, stopping modulating the current working frequency of the core 80.

[0385] The invention can modulate the frequency of the core 80 through the phase locked loops 70 shown in FIG. 2 or software. That is, according to the frequency modulation mechanism on a level of the cores, the core 80 is modulated to the suitable working frequency according to the actual computing performance of the core 80, the

frequency of the core 80 with high computing performance is modulated up, and the frequency of the core 80 with low computing performance is modulated down, thereby fully playing the computing performance of each core 80.

[0386] For example, the first correct ratio threshold and the second correct ratio threshold are both 90%. When the core 80 is worked at 600 MHz, if the computing correct ratio of the core 80 within the predetermined modulation period exceeds 90% (it shows that the core 80 does not reach the best computing performance), the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency, i.e., the working frequency is improved to 650 MHz. If the computing correct ratio of the core 80 is less than 90% (it shows that the computing performance of the core 80 is insufficient to work at the frequency of the current working frequency 600 MHz), the current working frequency of the core 80 is modulated down to the lower working frequency, i.e., the working frequency is reduced to 550 MHz. Those skilled in the art can understand that the upper working frequency is not limited to the upper adjacent working frequency, and one or more upper adjacent working frequencies also can be the upper working frequency; the lower working frequency is not limited to the lower adjacent working frequency, and one or more lower adjacent working frequencies also can be the lower working frequency. Preferably, a frequency difference between the current working frequency and the upper working frequency is from 1% to 10%, and a frequency difference between the current working frequency and the lower working frequency is from 1% to 10%, such that the core 80 is modulated up from the current working frequency to the upper working frequency or the lower working frequency, and benefit of the computing performance of the core 80 shall be greater than loss. That is, the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 700 MHz, the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 500 MHz, and so on.

Here, a spacing between the upper working frequency and the lower working frequency is not limited.

[0387] For another example, the first correct ratio threshold is 90%, and the second correct ratio threshold is 80%. If the core 80 is worked at 600 MHz, if the computing correct ratio of the core 80 within the predetermined modulation period exceeds 90% (it shows that the core 80 does not reach the best computing performance), the current working frequency of the core 80 is modulated up to the upper working frequency, i.e., the working frequency is improved to 650 MHz. If the computing correct ratio of the core 80 is less than 80% (it shows that the computing performance of the core 80 is insufficient to work at the frequency of the current working frequency 600 MHz), the current working frequency of the core 80 is modulated down to the lower working frequency, i.e., the working frequency is reduced to 550 MHz.

[0388] FIG. 11 is a flow diagram of a preferable chip frequency modulation method of a computing device in the second embodiment of the invention, which can be implemented by the chip frequency modulation apparatus 100 of the computing device shown in FIG. 3. The computing device comprises at least one operational chip, and the operational chip is provided with a plurality of cores. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. Preferably, the computing correct ratio can be a computing correct ratio of Nonces submitted by the core 80 within the modulation period. That is, during a predetermined time, in all Nonces submitted by the core 80, the computing correct ratio is a ratio occupied by correct Nonces. A block header in a blockchain comprises the Nonce (four bytes), Nonce is a random value, and the function of miners is actually to guess the value of Nonce, such that a hash of the block header can be less than a target value, and can be written into the blockchain. Specifically, this attribute starts from 0 to 2^{32} to compute the hash of the block header, and

if the obtained hash result conforms to conditions, mining is successful. The method comprises steps of:

[0389] Step S1101, setting a plurality of working frequencies for the operational chip of the computing device and causing the plurality of cores 80 in the operational chip to work at the respective working frequencies.

[0390] Step S1102, analyzing whether the Nonces submitted by the core 80 are correct within the modulation period.

[0391] Preferably, the step comprises:

[0392] (1) computing, via the core 80, a first result from the Nonce through a predetermined algorithm every time when the core 80 submits one Nonce within the modulation period, the first result including a first feature. The Nonce submitted by each core 80 includes identification information (ID) of Nonce, thereby counting the computing result of each core 80.

[0393] (2) computing, via a verification unit of the operational chip, a second result from the Nonce through the same algorithm, the second result including a second feature.

[0394] (3) if the first feature is the same as the second feature, judging, via the verification unit, that the Nonce is the correct Nonce, or the Nonce is the wrong Nonce.

[0395] For example, after the core 80 computes and submits one Nonce, the Nonce is embedded into the block header to compute a first hash result, and value of front twenty bits of the first hash result is 0 (the first feature). The first verification unit 212 also embeds the Nonce into the block header to compute a second hash result, and if value of front twenty bits of the second hash result is also 0 (the second feature), it is considered that the Nonce is one correct submission.

[0396] Step S1103, counting the number of correct Nonces and the number of wrong Nonces submitted by the core 80 within the modulation period;

[0397] Step S1104, computing a computing correct ratio of Nonces of the core 80 within the modulation period according to the number of correct Nonces and the number of wrong Nonces;

[0398] Step S1105, judging whether the computing correct ratio of Nonces reaches the predetermined first and/or second correct ratio thresholds, if the computing correct ratio of Nonces of the core 80 reaches the first correct ratio threshold, executing step S1106, and if the computing correct ratio of Nonces of the core 80 does not reach the second correct ratio threshold, executing step S1107;

[0399] Step S1106, if the computing correct ratio of Nonces of the core 80 reaches the first correct ratio threshold, modulating the current working frequency of the core 80 up to the upper working frequency;

[0400] Step S1107, if the computing correct ratio of Nonces of the core 80 does not reach the second correct ratio threshold, modulating the current working frequency of the core 80 down to the lower working frequency.

[0401] FIG. 12 is a flow diagram of a chip frequency modulation method of a computing device in the third embodiment of the invention, which can be implemented by the chip frequency modulation apparatus 100 of the computing device shown in FIG. 4. The computing device comprises at least one operational chip, and the operational chip is provided with a plurality of cores. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. The method comprises steps of:

[0402] Step S1201, setting a plurality of working frequencies for the operational chip of the computing device and causing the plurality of cores 80 in the operational chip to work at the respective working frequencies.

[0403] The step sets a plurality of working frequencies for each operational chip, and causes the plurality of cores 80 in the operational chip to work at the respective working

frequencies according to the frequency modulation mechanism on a level of the operational chip. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. The number of working frequencies and a distance between the frequencies in the invention can be set according to actual needs, and the more the working frequencies are, the most likely the computing performance of the respective cores 80 will be fully played. When a frequency modulation switch is turned on (without modulating the frequencies of the cores 80), the cores 80 can be evenly distributed, unevenly distributed or randomly distributed to work at the working frequencies depending on a predetermined rule. Preferably, the plurality of working frequencies can be set for the operational chip through a plurality of phase locked loops 70 shown in FIG. 2. Of course, the plurality of working frequencies also can be set for the operational chip through other hardware or software.

[0404] It shall be noticed that a frequency difference between the working frequencies in the invention shall be controlled within a reasonable range, because when the core 80 is improved by one working frequency, the working frequency of the core is improved by one frequency difference, thereby improving certain computing performance due to improvement of the computing speed. Meanwhile, improvement of the working frequency of the core may cause loss of certain computing performance due to reduction of the computing correct ratio. Therefore, the frequency setting module 10 shall reasonably control the frequency difference between the adjacent working frequencies, such that when the core 80 is modulated up from the current working frequency to the upper working frequency, benefit of the computing performance of the core 80 shall be greater than loss. Preferably, a frequency difference between the adjacent working frequencies is from 1% to 10%.

[0405] Step S1202, presetting a reference node value, a computing correct weight value, a computing wrong weight value, a computing correct threshold and a computing wrong threshold of the core 80.

[0406] Preferably, the computing correct weight value can be the same as or different from the computing wrong weight value, and the computing correct threshold can be the same as or different from the computing wrong threshold. The reference node value, the computing correct weight value, the computing wrong weight value, the computing correct threshold and the computing wrong threshold are all adjustable parameters, and can be optimized according to actual needs such as frequency modulation speed.

[0407] Preferably, the reference node value, the computing correct weight value, the computing wrong weight value, the computing correct threshold and/or the computing wrong threshold of the core 80 are set and adjusted according to actual requirements, the computing correct weight value is the same as or different from the computing wrong weight value, and the computing correct threshold is the same as or different from the computing wrong threshold.

[0408] An expected tolerant resident error ratio of the core 80 is controlled by controlling a ratio of the computing correct weight value to the computing wrong weight value. A computing formula of the resident error ratio is: the resident error ratio = the computing correct weight value divided by the computing correct weight value and the computing wrong weight value.

[0409] A modulation period is controlled by controlling an absolute value of the computing correct weight value and the computing wrong weight value.

[0410] The modulation period is controlled by controlling an absolute value of the computing correct threshold and the computing wrong threshold.

[0411] Step S1203, analyzing whether each computation of the core 80 is correct.

[0412] The core 80 can make various different computations to analyze whether one or more computations of the core 80 each time are correct. Preferably, whether the Nonces computed by the core 80 are correct is analyzed.

[0413] Step S1204, adding one computing correct weight value to the reference node value every time when the core 80 computes correctly at least once, and reducing one computing wrong weight value from the reference node value every time when the core 80 computes wrongly at least once. Preferably, one computing correct weight value is added to the reference node value every time when the core 80 computes correctly once. Of course, it can be set that one computing correct weight value is added to the reference node value every time when the core 80 computes correctly N (N is a natural number greater than 1) times. One computing wrong weight value is reduced from the reference node value every time when the core 80 computes wrongly once. Of course, it can be set that one computing wrong weight value is reduced from the reference node value every time when the core 80 computes wrongly N (N is a natural number greater than 1) times.

[0414] Step S1205, judging whether the current reference node value of the core 80 reaches the computing correct threshold or the computing wrong threshold, if the current reference node value of the core 80 reaches the computing correct threshold, executing step S1206, and if the current reference node value of the core 80 reaches the computing wrong threshold, executing step S1207.

[0415] Preferably, the step comprises:

[0416] (1) real-time judging whether the current reference node value of the core 80 reaches the computing correct threshold or the computing wrong threshold according to a preset real-time modulating instruction; or

[0417] (2) judging whether the current reference node value of the core 80 reaches the computing correct threshold or the computing wrong threshold according to a preset

timed modulating instruction within a modulation time period set by the timed modulating instruction; or

[0418] (3) analyzing whether the current reference node value of the core 80 reaches the computing correct threshold or the computing wrong threshold according to a received immediate modulating instruction.

[0419] Step S1206, if the current reference node value of the core 80 reaches the computing correct threshold, and shows that the core 80 does not reach the best computing performance, modulating the current working frequency of the core 80 up to the upper working frequency.

[0420] Preferably, the step comprises:

[0421] (1) if the current reference node value of the core 80 reaches the computing correct threshold, real-time modulating the current working frequency of the core 80 up to the upper working frequency; or

[0422] (2) if the current reference node value of the core 80 reaches the computing correct threshold in the modulation time period, modulating the current working frequency of the core 80 up to the upper working frequency; or

[0423] (3) according to the received immediate modulating instruction, if the current reference node value of the core 80 reaches the computing correct threshold, modulating the current working frequency of the core 80 up to the upper working frequency; according to a received stop modulating instruction, stopping modulating the current working frequency of the core 80.

[0424] Step S1207, if the current reference node value of the core 80 reaches the computing wrong threshold, and shows that the computing performance of the core 80 is insufficient to work at the current working frequency, modulating the current working frequency of the core 80 down to the lower working frequency.

[0425] Preferably, the step comprises:

[0426] (1) if the current reference node value of the core 80 reaches the computing wrong threshold, real-time modulating the current working frequency of the core 80 down to the lower working frequency; or

[0427] (2) if the current reference node value of the core 80 reaches the computing wrong threshold in the modulation time period, modulating the current working frequency of the core 80 down to the lower working frequency; or

[0428] (3) if the current reference node value of the core 80 reaches the computing wrong threshold, modulating the current working frequency of the core 80 down to the lower working frequency; according to a received stop modulating instruction, stopping modulating the current working frequency of the core 80.

[0429] For example, users can timely send the immediate modulating instruction to the computing device according to needs, and users add a weight A to the reference node every time when the core 80 computes the correct Nonce once, and reduce a weight B from the reference node every time when the core 80 computes the wrong Nonce once. When the currently added value reaches the computing correct number threshold C, the core 80 steps upward to the upper frequency. When the currently reduced value reaches the computing wrong number threshold D, the core 80 steps downward to the lower frequency. In addition, users can timely send stop modulating instruction to the computing device according to needs, and after receiving the stop modulating instruction, the computing device immediately stops modulating the frequency of the core 80.

[0430] Those skilled in the art can understand that the upper working frequency is not limited to the upper adjacent working frequency, and one or more upper adjacent working frequencies also can be the upper working frequency; the lower working frequency is not limited to the lower adjacent working frequency, and one or more lower adjacent

working frequencies also can be the lower working frequency. Preferably, a frequency difference between the current working frequency and the upper working frequency is from 1% to 10%, and a frequency difference between the current working frequency and the lower working frequency is from 1% to 10%, such that the core 80 is modulated up from the current working frequency to the upper working frequency or the lower working frequency, and benefit of the computing performance of the core 80 shall be greater than loss. That is, the current working frequency 600 MHz of the core 80 is modulated up to the upper working frequency 700 MHz, the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 500 MHz, and so on. Here, a spacing between the upper working frequency and the lower working frequency is not limited.

[0431] Preferably, the step can modulate the frequency of the core 80 through the phase locked loops 70 shown in FIG. 2 or software. That is, according to the frequency modulation mechanism on a level of the cores, the core 80 is modulated to the suitable working frequency according to the actual computing performance of the core 80, the frequency of the core 80 with high computing performance is modulated up, and the frequency of the core 80 with low computing performance is modulated down, thereby fully playing the computing performance of each core 80.

[0432] For example, as shown in FIG. 5, the reference node value is set to be 400,000, the computing correct weight value is set to be 180, the computing wrong weight value is set to be 9,000, and the computing correct threshold and the computing wrong threshold are both set to be 100,000.

[0433] 180 (the computing correct weight value) is added to the reference node value every time when the core 80 computes correctly at least once, 9,000 (the computing wrong weight value) is reduced from the reference node value every time when the core 80 computes wrongly at least once, and taking the reference node value for reference, the upper

frequency or the lower frequency is stepped upward or downward every time when 100,000 (the computing correct threshold and the computing wrong threshold) is added or reduced.

[0434] The current mechanism is similar with wrong or correct tug-of-war mechanism, correct and wrong mechanisms may have different weights. The reference node value is set. One computing correct weight value is added every time when one correct result is received, one computing wrong weight value is reduced every time when one wrong result is received, and if reward or punishment exceeds a corresponding threshold, the frequency is modulated up or down. It can be understood that the system has a marker, the reference node value is an initial value of the marker, maker + 180 for correct submission, and maker–9000 for each wrong submission. After Nth (N is a natural number greater than or equal to 1) corrects and Mth (M is a natural number greater than or equal to 1) errors, the marker shall be at a position of 400000 + N * 180–M*9000, and if the marker exceeds one threshold, the frequency is modulated correspondingly (modulating up or down). Then, every time when the frequency is modulated to a new frequency, the value is initialized, i.e., the current reference node value is reset to an initial reference node value.

[0435] FIG. 13 is a flow diagram of a preferable chip frequency modulation method of a computing device in the third embodiment of the invention, which can be implemented by the chip frequency modulation apparatus 100 of the computing device shown in FIG. 4. The computing device comprises at least one operational chip, and the operational chip is provided with a plurality of cores. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. The method comprises steps of:

[0436] Step S1301, setting a plurality of working frequency for the operational chip of the computing device and causing the plurality of cores 80 in the operational chip to work at the respective working frequencies;

[0437] Step S1302, presetting a reference node value, a computing correct weight value, a computing wrong weight value, a computing correct threshold and a computing wrong threshold of the core 80;

[0438] Step S1303, analyzing whether the Nonces submitted by the core 80 each time are correct.

[0439] Preferably, the step further comprises:

[0440] (1) computing, via the core 80, a first result from the Nonce through a predetermined algorithm after the core 80 submits one Nonce, the first result including a first feature;

[0441] (2) computing, via a verification unit of the operational chip, a second result from the Nonce through the same algorithm, the second result including a second feature.

[0442] (3) if the first feature is the same as the second feature, judging, via the verification unit, that the Nonce is the correct Nonce, or the Nonce is the wrong Nonce.

[0443] For example, after the core 80 computes and submits one Nonce, the Nonce is embedded into the block header to compute a first hash result, and value of front twenty bits of the first hash result is 0 (the first feature). The second verification unit 252 also embeds the Nonce into the block header to compute a second hash result, and if value of front twenty bits of the second hash result is also 0 (the second feature), it is considered that the Nonce is one correct submission.

[0444] Step S1304, adding one computing correct weight value to the reference node value every time when the core 80 submits at least one correct Nonce, and reducing one computing wrong weight value from the reference node value every time when the core 80 submits at least one wrong Nonce. Preferably, one computing correct weight value is added to the reference node value every time when the core 80 submits one correct Nonce. Of course, it also can be set that one computing correct weight value is added to the

reference node value every time when the core 80 submits Nth (N is a natural number greater than 1) correct Nonces. One computing wrong weight value is reduced from the reference node value every time when the core 80 submits one wrong Nonce. Of course, it also can be set that one computing wrong weight value is reduced from the reference node value every time when the core 80 submits Nth (N is a natural number greater than 1) wrong Nonces.

[0445] Step S1305, judging whether the current reference node value of the core 80 reaches the computing correct threshold or the computing wrong threshold, if the current reference node value of the core 80 reaches the computing correct threshold, executing step S1306, and if the current reference node value of the core 80 reaches the computing wrong threshold, executing step S1307.

[0446] Step S1306, if the current reference node value of the core 80 reaches the computing correct threshold, modulating the current working frequency of the core 80 up to the upper working frequency.

[0447] Step S1307, if the current reference node value of the core 80 reaches the computing wrong threshold, modulating the current working frequency of the core 80 down to the lower working frequency.

[0448] In one specific application embodiment of the invention, six phase locked loops 70 are used, and six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. As shown in FIG. 5, the reference node value is set to be 400,000, the computing correct weight value is set to be 180, the computing wrong weight value is set to be 9,000, and the computing correct threshold and the computing wrong threshold are both set to be 100,000.

[0449] The number of cores distributed at the respective corresponding frequencies as counted by four hash boards is as follows:

[0450] Hash board 0: [294 26 96 224 1023 1665]

[0451] Hash board 1: [274 47 111 212 963 1721]

[0452] Hash board 2: [350 25 153 369 1381 1050]

[0453] Hash board 3: [488 33 184 367 1342 950]

[0454] Firstly, the mechanism is further explained with reference to data. According to the resident error ratio S = the computing correct weight value divided by the computing correct weight value and the computing wrong weight value, the resident error ratio S (which is understood to long-term reside on one frequency) of the core 80 can be inferred to be 180/（180+9000）=1.29% through the given data. Accordingly, the core 80 is worked at one frequency for a long time (because a desired step is 0), and the working frequency is not modulated up or down. It can be inferred that if a computing error ratio of the core 80 is greater than 1.29% (the resident error ratio S), the working frequency is modulated up, and if a computing error ratio of the core 80 is less than 1.29% (the resident error ratio S), the working frequency is modulated down.

[0455] According to difficulty of settings (the difficulty is associated with a verification reference, and has influence on the computing correct ratio of the core 80, and the larger a coefficient of difficulty is, the lower the correct ratio will be; in contrast, the higher the correct ratio will be), a substantial period of modulation when error rises can be inferred. Assuming that an error ratio is e, the desired step of each Nonce is: (1-e)*180-e*9000=180-9180e. Taking e=0.5% for example, the desired step equals to 134.1, taking e=1% for example, the desired step equals to 88.2, and taking e=2% for example, the desired step equals to -3.6.

[0456] Computation is made using 650MHz, and an expectation of the single Nonce submitted by the core 80 is 1.3 per second (i.e., 1.3 Nonce is submitted within one second). Explanations are made using a scene where e is 0.5%, i.e., after 746 Nonces are

submitted, the expectation can be modulated up once. When e is 1.0%, 1134 Nonces are submitted, and the expectation is modulated up once; if the error ratio is 2.0%, 27,778 Nonces are submitted, the expectation is modulated down once, and so on.

[0457] FIG. 14 is a flow diagram of a chip frequency modulation method of a computing device in the fourth embodiment of the invention, which can be implemented by the chip frequency modulation apparatus 100 of the computing device. The computing device comprises at least one operational chip, and the operational chip is provided with a plurality of cores. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. The method comprises steps of:

[0458] Step S1401, setting a plurality of working frequency for the operational chip of the computing device and causing the plurality of cores 80 in the operational chip to work at the respective working frequencies.

[0459] The step sets a plurality of working frequencies for each operational chip, and causes the plurality of cores 80 in the operational chip to work at the respective working frequencies according to the frequency modulation mechanism on a level of the operational chip. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set. The number of working frequencies and a distance between the frequencies in the invention can be set according to actual needs, and the more the working frequencies are, the most likely the computing performance of the respective cores 80 will be fully played. When a frequency modulation switch is turned on (without modulating the frequencies of the cores 80), the cores 80 can be evenly distributed, unevenly distributed or randomly distributed to work at the working frequencies depending on a predetermined rule. The step can set the plurality of working frequencies for the operational chip through a plurality of phase locked loops 70 shown in FIG. 2. Of course, the method also can set the plurality of working frequencies for the operational chip through other hardware or software.

[0460] It shall be noticed that a frequency difference between the working frequencies in the invention shall be controlled within a reasonable range, because when the core 80 is improved by one working frequency, the working frequency of the core is improved by one frequency difference, thereby improving certain computing performance due to improvement of the computing speed. Meanwhile, improvement of the working frequency of the core may cause loss of certain computing performance due to reduction of the computing correct ratio. Therefore, the frequency setting module 10 shall reasonably control the frequency difference between the adjacent working frequencies, such that when the core 80 is modulated up from the current working frequency to the upper working frequency, benefit of the computing performance of the core 80 shall be greater than loss. Preferably, a frequency difference between the adjacent working frequencies is from 1% to 10%.

[0461] Step S1402, analyzing a computing performance indicator of each core 80 at its current working frequency.

[0462] The computing performance indicator represents the actual computing performance of the core 80 at the current working frequency, and includes, but is not limited to a computing correct ratio, a computing correct number, a computing speed and the like. If the computing performance indicator of the core 80 is high, it means that the computing performance of the core 80 may have room for improvement, and if the computing performance indicator of the core 80 is low, it means that the computing performance of the core 80 may be insufficient to work at the frequency corresponding to the current working frequency.

[0463] Step S1403, modulating the current working frequency of the core 80 up or down according to the computing performance indicator of the core 80.

[0464] According to the frequency modulation mechanism on a level of the cores, the step modulates the core 80 to the suitable working frequency according to the actual computing performance of the core 80, the frequency of the core 80 with high computing performance is modulated up, and the frequency of the core 80 with low computing performance is modulated down, thereby fully playing the computing performance of each core 80. The step can modulate the frequency of the core 80 through the phase locked loops 70 shown in FIG. 2 or software. Preferably, if the computing correct ratio of the core 80 within the modulation period reaches the first correct ratio threshold, it shows that the core 80 does not reach the best computing performance, so the current working frequency of the core 80 is modulated up to the upper working frequency. If the computing correct ratio of the core 80 within the modulation period does not reach the second correct ratio threshold, it shows that the computing performance of the core 80 is insufficient to work at the current working frequency, so the current working frequency of the core 80 is modulated down to the lower working frequency.

[0465] Those skilled in the art can understand that the upper working frequency is not limited to the upper adjacent working frequency, and one or more upper adjacent working frequencies also can be the upper working frequency; the lower working frequency is not limited to the lower adjacent working frequency, and one or more lower adjacent working frequencies also can be the lower working frequency. Preferably, a frequency difference between the current working frequency and the upper working frequency is from 1% to 10%, and a frequency difference between the current working frequency and the lower working frequency is from 1% to 10%, such that the core 80 is modulated up from the current working frequency to the upper working frequency or the lower working frequency, and benefit of the computing performance of the core 80 shall be greater than loss. That is, the current working frequency 600 MHz of the core 80 is modulated up to the upper

working frequency 700 MHz, the current working frequency 600 MHz of the core 80 is modulated down to the lower working frequency 500 MHz, and so on. Here, a spacing between the upper working frequency and the lower working frequency is not limited.

[0466] Step S1404, counting current distribution state of the cores 80 after frequency modulation at the respective working frequencies.

[0467] After the working frequency is automatically modulated according to the computing performance itself, the cores 80 are distributed to work at the respective working frequencies, and counting the distributed number of the cores 80 after frequency modulation at the respective working frequencies can obtain the current distribution state. Preferably, the working frequency can be divided to comprise at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, and the minimum frequency in the low-frequency working frequency is a minimum working frequency. For example, there are totally one thousand cores 80, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, and the number of cores 80 sequentially distributed at the six working frequencies is 100, 200, 100, 100, 200 and 300, respectively. 500 MHz and 550 MHz are low-frequency working frequencies, 600 MHz and 650 MHz are middle working frequencies, and 700 MHz and 750 MHz are high-frequency working frequency. 500 MHz is the minimum working frequency, and 750 MHz is the maximum working frequency.

[0468] Step S1405, modulating a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism, the frequency modulation mechanism being a correspondence relationship between the distribution state and the frequency modulation of the cores 80.

[0469] The frequency modulation mechanism is a correspondence relationship between the distribution state and the frequency modulation. The distribution state of the cores refers to a distribution state of the cores 80 worked at the respective working frequency. Modulating a frequency in the working frequency refers to directly modulate the frequency in the working frequency. Preferably, the frequency in the working frequency is modulated through the phase locked loops 70 shown in FIG. 2. An ideal state of the invention is to hope that over the predetermined ratio (e.g., 50%) or the maximum number of cores 80 falls into the middle working frequencies, such that the frequencies of the cores 80 have a large room for modulation up.

[0470] For example, if over the predetermined ratio (e.g., 30%) of cores 80 are worked at the high working frequency (750 MHz), it may cause that the cores 80 do not play the maximum computing performance (which may be higher), so one working frequency (600 MHz) is modified to at least one optimized high-frequency working frequency (800 MHz), and the cores 80 originally worked at the working frequency (600 MHz) are all transferred to work at the maximum working frequency (750 MHz). The frequency in the optimized high-frequency working frequency is higher than the frequency in the maximum working frequency, thereby fully playing the computing performance of the respective cores 80.

[0471] Preferably, after the step S1405, the method may further comprise:

[0472] if the cores 80 exceeding a predetermined fourth ratio are worked at the at least one middle working frequency, stopping modulating the frequency in the working frequency; or if the number of cores 80 worked at the at least one middle working frequency is maximum, stopping modulating the frequency in the working frequency. A relative ideal state is that over the predetermined fourth ratio (e.g., 50%) or the maximum number of the

cores 80 falls into one or more middle working frequencies, such as, the third working frequency (600 MHz), so frequency modulation of the cores 80 is unnecessary.

[0473] FIG. 15 is a flow diagram one of a preferable chip frequency modulation method of a computing device in the fourth embodiment of the invention, which can be implemented by the chip frequency modulation apparatus 100 of the computing device. The computing device comprises at least one operational chip, and the operational chip is provided with a plurality of cores. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. The method comprises steps of:

[0474] Step S1501, setting a plurality of working frequencies for the operational chip of the computing device and causing the plurality of cores 80 in the operational chip to work at the respective working frequencies;

[0475] Step S1502, analyzing a computing performance indicator of each core 80 at its current working frequency;

[0476] Step S1503, modulating the current working frequency of the core 80 up or down according to the computing performance indicator of the core 80;

[0477] Step S1504, counting current distribution state of the cores 80 after frequency modulation at the respective working frequencies. The working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency.

[0478] Step S1505, if the cores 80 exceeding a predetermined second ratio are worked at the at least one high-frequency working frequency, and may cause that the cores 80 do not play the maximum computing performance (which may be higher), modifying the at least one working frequency to at least one optimized high-frequency working frequency,

and a frequency in the optimized high-frequency working frequency is higher than a frequency in the maximum working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0479] For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, and if over 30% (the second ratio) of the cores 80 are worked at the two high-frequency working frequencies (700 MHz and 750 MHz), the two low-frequency working frequencies (500 MHz and 550 MHz) are modified to two optimized high-frequency working frequencies (800 MHz and 850 MHz), or one low-frequency working frequency (500 MHz) and one middle working frequency (600 MHz) are modified to two optimized high-frequency working frequencies (800 MHz and 850 MHz).

[0480] Preferably, if the cores 80 exceeding the second ratio are worked at the maximum working frequency, the step modifies the one working frequency to the one optimized high-frequency working frequency, and a frequency in the optimized high-frequency working frequency is higher than a frequency in the maximum working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0481] For example, if over 30% (the second ratio) of the cores 80 are worked at the maximum working frequency(750 MHz), one low-frequency working frequency (500 MHz) is modified to an optimized high-frequency working frequency (800 MHz), or one middle working frequency (600 MHz) is modified to an optimized high-frequency working frequency (800 MHz), or the maximum working frequency (750 MHz) is modified to an optimized high-frequency working frequency (800 MHz).

[0482] Step S1506, if the cores 80 exceeding a predetermined third ratio are worked at the at least one low-frequency working frequency, and means that the computing

capability of the cores 80 is too poor to be insufficient to work at the low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency, and a frequency in the optimized low-frequency working frequency is lower than a frequency in the minimum working frequency. It shall be noticed that the step can be omitted, i.e., the at least one working frequency is not modified to at least one optimized low-frequency working frequency.

[0483] The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency. For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, and if over 30% (the third ratio) of the cores 80 are worked at the two low-frequency working frequencies (500 MHz and 550 MHz), the two low-frequency working frequencies (500 MHz and 550 MHz) are modified to two optimized low-frequency working frequencies (400 MHz and 450 MHz), or one low-frequency working frequency (500 MHz) and one middle working frequency (600 MHz) are modified to two optimized low-frequency working frequencies (400 MHz and 450 MHz).

[0484] Preferably, if the cores 80 exceeding the third ratio are worked at the minimum working frequency, the step modifies the one working frequency to the one optimized low-frequency working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency. For example, if over 30% (the third ratio) of the cores 80 are worked at the minimum working frequency (500 MHz), one low-frequency working frequency (500 MHz) is modified to an optimized low-frequency working frequency (450 MHz), or one middle working frequency (600 MHz) is modified to an optimized low-frequency working frequency (450 MHz), or the maximum working frequency (750 MHz) is modified to an optimized low-frequency working frequency (450 MHz)

[0485] Preferably, after the step S1506, the method further comprises:

[0486] if the cores 80 exceeding a predetermined fourth ratio are worked at the at least one middle working frequency, stopping modulating the frequency in the working frequency, because a relative ideal state is that over the predetermined fourth ratio (e.g., 50%) of the cores 80 falls into one or more middle working frequencies, such as, the third working frequency (600 MHz), which can fully play the working performance of the cores 80, so frequency modulation of the cores 80 is unnecessary.

[0487] if the number of cores 80 worked at the at least one middle working frequency is maximum, stopping modulating the frequency in the working frequency, because a relative ideal state is that the maximum number of the cores 80 falls into one or more middle working frequencies, such as, the third working frequency (600 MHz), which can fully play the working performance of the cores 80, so frequency modulation of the cores 80 is unnecessary.

[0488] In one specific application embodiment of the invention, six phase locked loops 70 are used, and six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set.

[0489] The number of cores distributed at the respective corresponding frequencies as counted by four hash boards is as follows:

[0490] Hash board 0: [294 26 96 224 1023 1665]

[0491] Hash board 1: [274 47 111 212 963 1721]

[0492] Hash board 2: [350 25 153 369 1381 1050]

[0493] Hash board 3: [488 33 184 367 1342 950]

[0494] Taking the four hash boards 0-3 for example, as shown in FIG. 7, data substantially conforms to a normal distribution, and the minimum working frequency (500 MHz) is the minimum frequency where the single core 80 is worked, and is unable to be

modulated down (if the error ratio is too high, it can consider closing the minimum frequency). If over the predetermined ratio (e.g., 50%) of the cores 80 are accumulated at the maximum working frequency (750 MHz), it means not playing the maximum efficiency (which may be higher), and the entire operational chip has further room for improvement. A relative ideal state is that over the predetermined ratio (e.g., 50%) or the maximum number of cores 80 falls into one or more middle working frequencies, such as, the third working frequency (600 MHz). To fully use the computing performance of the cores 80, a long tail at the high performance side, rather than a long tail at the low frequency, shall be considered.

[0495] Taking the hash boards 0-1 for example, it can be seen that if the frequency 600 MHz is removed, and if left shift as a whole is used, generally, one hundred cores 80 fall at the frequency 550 MHz, and the current frequency is obviously in a left low-frequency region, which does not facilitate fully playing the computing performance of the cores 80. Therefore, right shift as a whole is more suitable, i.e., a whole shifting way. If the frequency 550 MHz is set to right as a whole to above the frequency 800 MHz through the phase locked loops 70, it is expected that several hundreds of the cores 80 are improved over 800 MHz, thereby improving the overall computing performance.

[0496] FIG. 16 is a flow diagram two of a preferable chip frequency modulation method of a computing device in the fourth embodiment of the invention, which can be implemented by the chip frequency modulation apparatus 100 of the computing device. The computing device comprises at least one operational chip, and the operational chip is provided with a plurality of cores. The computing device is preferably for mass operation, such as, operation of mining virtual digital currency. The method comprises steps of:

[0497] Step S1601, setting a plurality of working frequencies for the operational chip of the computing device and causing the plurality of cores 80 in the operational chip to work at the respective working frequencies;

[0498] Step S1602, analyzing a computing performance indicator of each core 80 at its current working frequency;

[0499] Step S1603, modulating the current working frequency of the core 80 up or down according to the computing performance indicator of the core 80;

[0500] Step S1604, counting current distribution state of the cores 80 after frequency modulation at the respective working frequencies. The working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency.

[0501] Step S1605, if the number of cores 80 worked at the at least one high-frequency working frequency is maximum, and may cause that the cores 80 do not play the maximum computing performance (which may be higher), modifying the at least one working frequency to at least one optimized high-frequency working frequency, and a frequency in the optimized high-frequency working frequency is higher than a frequency in the maximum working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0502] For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, and the maximum number of the cores 80 is worked at the two high-frequency working frequencies (700 MHz and 750 MHz), so the two low-frequency working frequencies (500 MHz and 550 MHz) are modified to two optimized high-frequency working frequencies (800 MHz and 850 MHz), or one low-frequency working frequency (500 MHz) and one middle working frequency (600 MHz) are modified to two optimized high-frequency working frequencies (800 MHz and 850 MHz).

[0503] Preferably, if the number of cores 80 worked at the maximum working frequency is maximum, the step modifies the one working frequency to the one optimized high-frequency working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0504] For example, when the maximum number of the cores 80 are worked at the maximum working frequency (750 MHz), one low-frequency working frequency (500 MHz) is modified to an optimized high-frequency working frequency (800 MHz), or one middle working frequency (600 MHz) is modified to an optimized high-frequency working frequency (800 MHz), or the maximum working frequency (750 MHz) is modified to an optimized high-frequency working frequency (800 MHz).

[0505] Step S1606, if the number of cores 80 worked at the at least one low-frequency working frequency is maximum, and means that the computing capability of the cores 80 is too poor to be insufficient to work at the low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency, and a frequency in the optimized low-frequency working frequency is lower than a frequency in the minimum working frequency, thereby avoiding the cores 80 with poor computing capability from influencing on the overall computing performance of the operational chip. The step can be omitted, i.e., the at least one working frequency is not modified to at least one optimized low-frequency working frequency.

[0506] The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency.

[0507] For example, six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set, and the maximum number of the cores 80 is worked at the two low-frequency working frequencies (500 MHz and 550 MHz), so the two low-

frequency working frequencies (500 MHz and 550 MHz) are modified to two optimized low-frequency working frequencies (400 MHz and 450 MHz), or one low-frequency working frequency (500 MHz) and one middle working frequency (600 MHz) are modified to two optimized low-frequency working frequencies (400 MHz and 450 MHz).

[0508] Preferably, if the number of cores 80 worked at the minimum working frequency is maximum, the step modifies the one working frequency to the one optimized low-frequency working frequency. The modified working frequency can be a low-frequency working frequency, a middle working frequency and/or a high-frequency working frequency. For example, when the maximum number of the cores 80 are worked at the minimum working frequency (500 MHz), one low-frequency working frequency (500 MHz) is modified to an optimized low-frequency working frequency (450 MHz), or one middle working frequency (600 MHz) is modified to an optimized low-frequency working frequency (450 MHz), or the maximum working frequency (750 MHz) is modified to an optimized low-frequency working frequency (450 MHz).

[0509] Preferably, after the step S1606, the method further comprises:

[0510] if the cores 80 exceeding a predetermined fourth ratio are worked at the at least one middle working frequency, stopping modulating the frequency in the working frequency; or

[0511] if the number of cores 80 worked at the at least one middle working frequency is maximum, stopping modulating the frequency in the working frequency.

[0512] In one specific application embodiment of the invention, six phase locked loops 70 are used, and six working frequencies 500 MHz, 550 MHz, 600 MHz, 650 MHz, 700 MHz and 750 MHz are set.

[0513] The number of cores distributed at the respective corresponding frequencies as counted by four hash boards is as follows:

[0514] Hash board 0: [294 26 96 224 1023 1665]

[0515] Hash board 1: [274 47 111 212 963 1721]

[0516] Hash board 2: [350 25 153 369 1381 1050]

[0517] Hash board 3: [488 33 184 367 1342 950]

[0518] Taking the four hash boards 0-3 for example, as shown in FIG. 7, data substantially conforms to a normal distribution, and the minimum working frequency (500 MHz) is the minimum frequency where the single core 80 is worked, and is unable to be modulated down (if the error ratio is too high, it can consider closing the minimum frequency). If the number of cores 80 accumulated at the maximum working frequency (750 MHz) is maximum, it means not playing the maximum efficiency (which may be higher), and the entire operational chip has further room for improvement. A relative ideal state is that over the predetermined ratio (e.g., 50%) or the maximum number of cores 80 falls into one or more middle working frequencies, such as, the third working frequency (600 MHz). To fully use the computing performance of the cores 80, a long tail at the high performance side, rather than a long tail at the low frequency, shall be considered.

[0519] Taking the hash boards 0-1 for example, it can be seen that if the frequency 600 MHz is removed, generally, one hundred cores 80 fall at the frequency 550 MHz, and the current frequency is obviously in a left low-frequency region. Therefore, right shift as a whole is more suitable, i.e., a whole shifting way. If the frequency 550 MHz is set to right as a whole to above the frequency 800 MHz through the phase locked loops 70, it is expected that several hundreds of the cores 80 are improved over 800 MHz, thereby improving the overall computing performance

[0520] The invention further provides a storage medium for storing a computer program executing the chip frequency modulation method of the computing device in any one of FIGS. 8 to 16. For example, when computer program instructions are executed by

computers, the method and/or the technical solution of the application can be invoked or provided through operation of the computers. Moreover, the program instructions for invoking the method of the application may be stored in a fixed or removable storage medium, and/or transmitted and/or stored in a storage of the computing device run by the program instructions through broadcast or data flow in other signal carrier media. Herein, according to that one embodiment of the application comprises one computing device shown in FIG. 17, the computing device preferably comprises a control board, and at least one hash board connected to the control board. The control board is provided with a processor, the hash board is provided with a plurality of operational chips for operation, and the operational chips are provided with a plurality of cores. The device comprises a storage medium for storing computer program instructions and a processor for executing the program instructions. When the computer program instructions are executed by the processor, the computing device is triggered to execute the method and/or the technical solution in the foregoing multiple embodiments.

[0521] It shall be noticed that the application is implementable in software and/or a combination of software and hardware. For example, the application is implementable in application-specific integrated circuits (ASICs), general-purpose computers or any other similar hardware equipment. In one embodiment, the software program of the application can be executed by the processor to implement the foregoing steps or functions. Similarly, the software program (including relevant data structure) of the application can be stored in a computer readable recording medium, such as, RAM memory, magnetic or optical driver, or floppy disk, or similar equipment. In addition, some steps or functions of the application are implementable using hardware, such as, circuits working together with the processor to execute the respective steps or functions.

[0522] The method of the invention can be implemented as a computer implementing method on computers, or special hardware, or a combination thereof. Executable codes or portions according to the method of the invention can be stored on computer program products. Examples of the computer program products include storage devices, optical storage devices, integrated circuits, servers, online software, and the like. Preferably, the computer program products include non-temporary program code units stored on a computer readable medium for executing the method of the invention when the program products are executed on the computers.

[0523] In one preferable embodiment, the computer program comprises computer program code units suitable for executing all steps in the method of the invention when the computer program is run on the computers. Preferably, the computer program is embodied on the computer readable medium.

[0524] To sum up, the invention automatically modulates frequencies of the cores of the operational chip of the computing device, firstly sets a plurality of suitable working frequencies and causes the plurality of cores in the operational chip to work at the respective working frequencies, and then modulates the current working frequency of the core up or down according to the computing performance indicator of each core at the current working frequency, that is, modulating the core with high computing performance up, and modulating the core with low computing performance down. Therefore, the invention can automatically modulate a frequency corresponding to each core according to the actual computing performance of each core in the operational chip of the computing device, thereby maximizing the computing performance of the cores and improving the operational performance of the operational chip and the overall operational device.

[0525] Of course, the invention also may have various other embodiments, and those skilled in the art shall make various corresponding modifications and variations

according to the invention without departing from spirit and essence of the invention, but these corresponding modifications and variations shall belong to the scope protected by the appended claims of the invention.

Industrial Applicability

[0526] Application of the chip frequency modulation method and apparatus of the computing device, the hash board, the computing device and the storage medium of the invention has the following advantageous effects:

[0527] automatically modulating a frequency corresponding to each core according to the actual computing performance of each core in the operational chip of the computing device, thereby maximizing the computing performance of the cores and improving the operational performance of the operational chip and the overall operational device.

WHAT IS CLAIMED IS:

1. A chip frequency modulation method of a computing device, the computing device provided with at least one operational chip, and the operational chip provided with a plurality of cores, comprising steps of:

setting a plurality of working frequencies of each of the plurality of cores the operational chip of the computing device and causing each of the plurality of cores in the operational chip to work at a current working frequency to compute one or more Nonces, wherein the current working frequency is one of the plurality of working frequencies;

receiving, from each of the plurality of cores, the one or more Nonces computed at the current working frequency;

for each of the plurality of cores, analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency; and

for at least one of the plurality of cores, modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator;

wherein the step of analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency further comprises:

presetting a reference node value, a computing correct weight value, a computing wrong weight value, a computing correct threshold and a computing wrong threshold of the core;

analyzing whether each computation of the at least one core is correct;

adding a computing correct weight value to a reference node value every time when the at least one core computes correctly at least once, and deducting a computing wrong

weight value from the reference node value every time when the at least one core computes wrongly at least once;

judging whether a current reference node value of the at least one core reaches a computing correct threshold or a computing wrong threshold;

the step of modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator further comprises:

if the current reference node value reaches the computing correct threshold, modulating the current working frequency of the core up to an upper working frequency of the plurality of working frequencies that is higher than the current working frequency; or;

if the current reference node value reaches the computing wrong threshold, modulating the current working frequency of the core down to a lower working frequency of the plurality of working frequencies that is lower than the current working frequency.

2. The chip frequency modulation method according to claim 1, wherein the step of setting a plurality of working frequencies of each of the plurality of cores the operational chip of the computing device and causing each of the plurality of cores in the operational chip to work at a current working frequencies further comprises:

setting the plurality of working frequencies for the operational chip through a plurality of phase locked loops, the working frequencies and the phase locked loops being in a one-to-one correspondence relationship;

the step of modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher

or lower than the current working frequency according to the computing performance indicator further comprises:

modulating the current working frequency up or downthrough the phase locked loops according to the computing performance indicator .

3. The chip frequency modulation method according to claim 2, wherein the phase locked loops are provided inside or outside the operational chip.

4. The chip frequency modulation method according to claim 1, wherein a frequency difference between the adjacent working frequencies is from 1% to 10%.

5. The chip frequency modulation method according to claim 1, further comprising:

if a portion of the cores worked at one or more optimized working frequencies exceed a first ratio, stopping modulating frequencies of the cores; or

if a portion of the cores worked at the one or more optimized working frequencies is majority, stopping modulating the frequencies of the cores.

6. The chip frequency modulation method according to claim 1, wherein the step of analyzing whether each computation of the at least one core is correct further comprises:

analyzing whether the random numbers submitted every time by the at least one core are correct;

the step of adding one computing correct weight value to the reference node value every time when the at least one core computes correctly at least once, and reducing one computing wrong weight value from the reference node value every time when the core computes wrongly at least once further comprises:

adding one computing correct weight value to the reference node value every time when the core submits at least one correct random number, and reducing one computing wrong weight value from the reference node value every time when the at least one core submits at least one wrong random number.

7. The chip frequency modulation method according to claim 6, wherein the step of analyzing whether the random numbers submitted every time by the at least one core are correct further comprises:

computing, via the at least one core, a first result from the random numbers through a predetermined algorithm after the core submits one random number, the first result including a first feature;

computing, via a verification unit of the operational chip, a second result from the random numbers through the same algorithm, the second result including a second feature;

if the first feature is the same as the second feature, judging, via the verification unit, that the random numbers are the correct random numbers, or the random numbers are the wrong random numbers.

8. The chip frequency modulation method according to claim 1, wherein the method further comprises:

setting and adjusting the reference node value, the computing correct weight value, the computing wrong weight value, the computing correct threshold and/or the computing

wrong threshold according to actual requirements, the computing correct weight value being the same as or different from the computing wrong weight value, the computing correct threshold being the same as or different from the computing wrong threshold;

controlling an expected tolerant resident error ratio by controlling a ratio of the computing correct weight value to the computing wrong weight value;

controlling a modulation period by controlling an absolute value of the computing correct weight value and the computing wrong weight value;

controlling the modulation period by controlling an absolute value of the computing correct threshold and the computing wrong threshold.

9. The chip frequency modulation method according to claim 8, wherein a computing formula of the resident error ratio is: the resident error ratio = the computing correct weight value divided by the computing correct weight value and the computing wrong weight value.

10. The chip frequency modulation method according to claim 1, wherein the step of judging whether a current reference node value of the at least one core reaches a computing correct threshold or a computing wrong threshold further comprises:

real-time judging whether the current reference node value of the at least one core reaches the computing correct threshold or the computing wrong threshold according to a preset real-time modulating instruction;

judging whether the current reference node value of the at least one core reaches the computing correct threshold or the computing wrong threshold according to a preset timed modulating instruction within a modulation time period set by the timed modulating instruction; or

analyzing whether the current reference node value reaches the computing correct threshold or the computing wrong threshold according to a received immediate modulating instruction;

the step of modulating the current working frequency up or down according to the computing performance indicator further comprises:

if the current reference node value of the at least one core reaches the computing correct threshold, real-time modulating the current working frequency up to the upper working frequency; if the current reference node value reaches the computing wrong threshold, real-time modulating the current working frequency down to the lower working frequency;

if the current reference node value reaches the computing correct threshold in the modulation time period, modulating the current working frequency up to the upper working frequency; if the current reference node value reaches the computing wrong threshold in the modulation time period, modulating the current working frequency down to the lower working frequency; or

according to the received immediate modulating instruction, if the current reference node value reaches the computing correct threshold, modulating the current working frequency up to the upper working frequency; if the current reference node value reaches the computing wrong threshold, modulating the current working frequency down to the lower working frequency; according to a received stop modulating instruction, stopping modulating the current working frequency .

11. The chip frequency modulation method according to claim 1, after the step of modulating the current working frequency up or down to a different working frequency of

the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator , further comprising:

counting current distribution state after frequency modulation at the working frequencies;

modulating a frequency in the working frequency according to the current distribution state and a frequency modulation mechanism of the cores, the frequency modulation mechanism being a correspondence relationship between the distribution state and the frequency modulation of the cores.

12. The chip frequency modulation method according to claim 11, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency;

the step of modulating a frequency in the working frequency according to the current distribution state and a frequency modulation mechanism of the cores further comprises:

if the cores exceeding a second ratio are worked at the at least one high-frequency working frequency, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

if the cores exceeding a third ratio are worked at the at least one low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

13. The chip frequency modulation method according to claim 12, wherein the step of if the cores exceeding the second ratio are worked at the at least one high-frequency working frequency, modifying the at least one working frequency to at least one optimized high-frequency working frequency further comprises:

if the cores exceeding the second ratio are worked at the maximum working frequency, modifying the one working frequency to the one optimized high-frequency working frequency; and/or

the step of if the cores exceeding the third ratio are worked at the at least one low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency further comprises:

if the cores exceeding the third ratio are worked at the minimum working frequency, modifying the one working frequency to the one optimized low-frequency working frequency.

14. The chip frequency modulation method according to claim 11, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency;

the step of modulating a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism further comprises:

if the number of cores worked at the at least one high-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized high-

frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

if the number of cores worked at the at least one low-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

15. The chip frequency modulation method according to claim 14, wherein the step of if the number of cores worked at the at least one high-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized high-frequency working frequency further comprises:

if the number of cores worked at the maximum working frequency is maximum, modifying the one working frequency to the one optimized high-frequency working frequency; and/or

the step of if the number of cores worked at the at least one low-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized low-frequency working frequency further comprises:

if the number of cores worked at the minimum working frequency is maximum, modifying the one working frequency to the one optimized low-frequency working frequency.

16. The chip frequency modulation method according to claim 11, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency;

the step of modulating a frequency in the working frequency according to the current distribution state and a frequency modulation mechanism further comprises:

if the cores exceeding the fourth ratio are worked at the at least one middle working frequency, stopping modulating the frequency in the working frequency; or

if the number of cores worked at the at least one middle working frequency is maximum, stopping modulating the frequency in the working frequency.

17. A chip frequency modulation apparatus of a computing device, the computing device provided with at least one operational chip, and the operational chip provided with a plurality of cores, comprising:

a frequency setting module for setting a plurality of working frequencies of each of the plurality of cores of the operational chip of the computing device and causing each of the plurality of cores in the operational chip to work a current working frequency to compute one or more Nonces,wherein the current working frequency is one of the plurality of working frequencies;

receiving,from each of the plurality of cores,the one or more Nonces computed at the current working frequency;

a computational performance analysis module for for each of the plurality of cores,analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency; and

a frequency modulation module for for at least one of the plurality of cores, modulating the current working frequency of the at least one core up or down to a different

working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator;

wherein the computational performance analysis module further comprises:

a setting sub-module for presetting a reference node value, a computing correct weight value, a computing wrong weight value, a computing correct threshold and a computing wrong threshold of the core;

a second analysis sub-module for analyzing whether each computation of the at least one core is correct;

a counting sub-module for adding a computing correct weight value to a reference node value every time when the at least one core computes correctly at least once, and deducting computing wrong weight value from the reference node value every time when the at least one core computes wrongly at least once; and

a second judgment sub-module for judging whether the current reference node value of at least one the core reaches the computing correct threshold or a computing wrong threshold;

the frequency modulation module for if the current reference node value reaches the computing correct threshold, modulating the current working frequency of the core up to the upper working frequency of the plurality of working frequencies that is higher than the current working frequency; and if the current reference node value reaches the computing wrong threshold, modulating the current working frequency of the core down to the lower working frequency of the plurality of working frequencies that is lower than the current working frequency .

18. The chip frequency modulation apparatus according to claim 17, wherein the frequency setting module sets the plurality of working frequencies for the operational chip

through a plurality of phase locked loops, the working frequencies and the phase locked loops being in a one-to-one correspondence relationship;

the frequency modulation module modulates the current working frequency up or down through the phase locked loops according to the computing performance indicator .

19. The chip frequency modulation apparatus according to claim 18, wherein the phase locked loops are provided inside or outside the operational chip.

20. The chip frequency modulation apparatus according to claim 17, wherein a frequency difference between the adjacent working frequencies is from 1% to 10%.

21. The chip frequency modulation apparatus according to claim 17, wherein the frequency modulation module further comprises:

a frequency modulation sub-module for modulating the current working frequency up or down according to the computing performance indicator ;

a stop frequency modulation sub-module for when a portion of if the cores worked at the predetermined one or more optimized working frequency exceed a first ratio, stopping modulating the frequencies of the cores; or if when a portion of the number of cores worked at the at least one optimized working frequencies is majority, stopping modulating the frequencies of the cores.

22. The chip frequency modulation apparatus according to claim 17, wherein the second analysis sub-module analyzes whether the random numbers submitted every time by the core are correct;

the counting sub-module adds one computing correct weight value to the reference node value every time when the core submits at least one correct random number, and reduces one computing wrong weight value from the reference node value every time when the core submits at least one wrong random number.

23. The chip frequency modulation apparatus according to claim 22, wherein the second analysis sub-module further comprises:

a second computing unit for computing, via the core, a first result from the random number through a predetermined algorithm after the core submits one random number, the first result including a first feature; and

a second verification unit for computing a second result from the random number through the same algorithm, the second result including a second feature; if the first feature is the same as the second feature, judging that the random number is the correct random number, or the random number is the wrong random number.

24. The chip frequency modulation apparatus according to claim 17, wherein the setting sub-module sets and adjusts the reference node value, the computing correct weight value, the computing wrong weight value, the computing correct threshold and/or the computing wrong threshold according to actual requirements, the computing correct weight value being the same as or different from the computing wrong weight value, the computing correct threshold being the same as or different from the computing wrong threshold;

the setting sub-module controls an expected tolerant resident error ratio by controlling a ratio of the computing correct weight value to the computing wrong weight value;

the setting sub-module controls a modulation period by controlling an absolute value of the computing correct weight value and the computing wrong weight value;

the setting sub-module controls the modulation period by controlling an absolute value of the computing correct threshold and the computing wrong threshold.

25. The chip frequency modulation apparatus according to claim 24, wherein a computing formula of the resident error ratio is: the resident error ratio = the computing correct weight value divided by the computing correct weight value and the computing wrong weight value.

26. The chip frequency modulation apparatus according to claim 17, wherein the computational performance analysis module real-time judges whether the current reference node value reaches the computing correct threshold or the computing wrong threshold according to a preset real-time modulating instruction;

the computational performance analysis module judges whether the current reference node value reaches the computing correct threshold or the computing wrong threshold according to a preset timed modulating instruction within a modulation time period set by the timed modulating instruction; or

the computational performance analysis module analyzes whether the current reference node value reaches the computing correct threshold or the computing wrong threshold according to a received immediate modulating instruction;

the frequency modulation module, if the current reference node value reaches the computing correct threshold, real-time modulates the current working frequency up to the

upper working frequency; if the current reference node value reaches the computing wrong threshold, real-time modulates the current working frequency down to the lower working frequency;

the frequency modulation module, if the current reference node value reaches the computing correct threshold in the modulation time period, modulates the current working frequency up to the upper working frequency; if the current reference node value reaches the computing wrong threshold in the modulation time period, modulates the current working frequency down to the lower working frequency; or

the frequency modulation module, according to the received immediate modulating instruction, if the current reference node value reaches the computing correct threshold, modulates the current working frequency up to the upper working frequency; if the current reference node value reaches the computing wrong threshold, modulates the current working frequency of the at least one core down to the lower working frequency; according to a received stop modulating instruction, stops modulating the current working frequency of the core.

27. The chip frequency modulation apparatus according to claim 17, further comprising:

a frequency counting module for counting current distribution state of the cores after frequency modulation at the working frequencies;

a frequency modulation module for modulating a frequency in the working frequency according to the current distribution state and a predetermined frequency modulation mechanism of the cores, the frequency modulation mechanism being a correspondence relationship between the distribution state and the frequency modulation of the cores.

28. The chip frequency modulation apparatus according to claim 27, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency;

the frequency modulation module further comprises:

a first frequency modulation sub-module for if the cores exceeding a second ratio are worked at the at least one high-frequency working frequency, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

a second frequency modulation sub-module for if the cores exceeding a third ratio are worked at the at least one low-frequency working frequency, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

29. The chip frequency modulation apparatus according to claim 28, wherein if the cores exceeding the second ratio are worked at the maximum working frequency, the first frequency modulation sub-module modifies the one working frequency to the one optimized high-frequency working frequency; and/or

if the cores exceeding the third ratio are worked at the minimum working frequency, the second frequency modulation sub-module modifies the one working frequency to the one optimized low-frequency working frequency.

30. The chip frequency modulation apparatus according to claim 27, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency, the maximum frequency in the high-frequency working frequency is a maximum working frequency, the minimum frequency in the low-frequency working frequency is a minimum working frequency;

the frequency modulation module further comprises:

a third frequency modulation sub-module for if the number of cores worked at the at least one high-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized high-frequency working frequency, a frequency in the optimized high-frequency working frequency being higher than a frequency in the maximum working frequency; and/or

a fourth frequency modulation sub-module for if the number of cores worked at the at least one low-frequency working frequency is maximum, modifying the at least one working frequency to at least one optimized low-frequency working frequency, a frequency in the optimized low-frequency working frequency being lower than a frequency in the minimum working frequency.

31. The chip frequency modulation apparatus according to claim 30, wherein if the number of cores worked at the maximum working frequency is maximum, the third frequency modulation sub-module modifies the one working frequency to the one optimized high-frequency working frequency; and/or

if the number of cores worked at the minimum working frequency is maximum, the fourth frequency modulation sub-module modifies the one working frequency to the one optimized low-frequency working frequency.

32. The chip frequency modulation apparatus according to claim 27, wherein the working frequency comprises at least one high-frequency working frequency, at least one middle working frequency and at least one low-frequency working frequency;

the frequency modulation module further comprises:

a first stop modulation module for if the cores exceeding a fourth ratio are worked at the at least one middle working frequency, stopping modulating the frequency in the working frequency; or

a second stop modulation module for if the number of cores worked at the at least one middle working frequency is maximum, stopping modulating the frequency in the working frequency.

33. The chip frequency modulation apparatus according to claim 17, wherein the chip frequency modulation apparatus is provided inside or outside the operational chip.

34. A hash board comprising the chip frequency modulation apparatus according to any one of claims 17 to 33.

35. A computing device comprising the chip frequency modulation apparatus according to any one of claims 17 to 33.

36. A computer program storage medium for storing a computer program, wherein when executed by a processor, the program implements a chip frequency modulation method of a computing device, the computing device provided with at least one operational chip, and the operational chip provided with a plurality of cores, wherein the method comprises:

setting a plurality of working frequencies of each of the plurality of cores of the operational chip of the computing device and causing each of the plurality of cores in the operational chip to work at a current working frequency to compute one or more Nonces, wherein the current working frequency is one of the plurality of working frequencies;

receiving, from each of the plurality of cores, the one or more Nonces computed at the current working frequency;

for each of the plurality of cores, analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency; and

for at least one of the plurality of cores, modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator;

wherein the step of analyzing a computing performance indicator of correctness of the one or more Nonces computed at the current working frequency further comprises:

presetting a reference node value, a computing correct weight value, a computing wrong weight value, a computing correct threshold and a computing wrong threshold of the core;

analyzing whether each computation of the at least one core is correct;

adding a computing correct weight value to a reference node value every time when the at least one core computes correctly at least once, and deducting a computing wrong

weight value from the reference node value every time when the at least one core computes wrongly at least once;

judging whether a current reference node value of the at least one core reaches a computing correct threshold or a computing wrong threshold;

the step of modulating the current working frequency of the at least one core up or down to a different working frequency of the plurality of working frequencies that is higher or lower than the current working frequency according to the computing performance indicator further comprises:

if the current reference node value reaches the computing correct threshold, modulating the current working frequency of the core up to an upper working frequency of the plurality of working frequencies that is higher than the current working frequency; or

if the current reference node value reaches the computing wrong threshold, modulating the current working frequency of the core down to a lower working frequency of the plurality of working frequencies that is lower than the current working frequency.