

CLAIMS

1. A data storage management apparatus, comprising:
at least two random access memories (RAMs);
a control unit, configured to receive an instruction, and generate and send a control
5 signal according to the instruction; and
a direct memory access controller (DMAC), configured to access data in the
RAMs according to the control signal;

~~2. The apparatus according to claim 1, wherein the DMAC configured to access
data in the RAMs according to the control signal, comprising:~~

10 the DMAC is further configured to read data from an external storage unit and
store the data in the RAM indicated by the control signal, according to the control signal;
or

the DMAC is further configured to read data from the RAM indicated by the
control signal and store the data in the external storage unit, according to the control
15 signal.

~~32. The apparatus according to claim 1-or-2, wherein the number of the RAM
indicated by the control signal is one or more.~~

~~43. The apparatus according to any one of claims 1-3claim 1 or 2, wherein all the
RAMs and an-the external storage unit are uniformly addressed; or, all the RAMs are
20 uniformly addressed.~~

~~54. The apparatus according to any one of claims 1-43, wherein an address range
accessible by the DMAC is address segments of all the RAMs and address segment of
the external storage unit.~~

~~65. A processing core, comprising a processing unit, a storage unit and the data
25 storage management apparatus according to any one of claims 1-54; wherein~~

the processing unit is configured to send an instruction, and the instruction is for
instructing the data storage management apparatus to access data in the storage unit;
and

the processing unit is further configured to read data required for executing a
30 program from any of the RAMs.

~~76. The processing core according to claim 65, wherein
the instruction includes a fetch instruction and a store instruction; and~~

the processing unit is configured to send the fetch instruction, and the fetch instruction is for instructing the data storage management apparatus to fetch data from the storage unit and store the data to a RAM indicated by the fetch instruction.

87. The processing core according to claim 76, wherein the DMAC is configured to, after completing the fetch instruction, send a storage completion signal; and the processing unit is configured to issue a new fetch instruction according to the storage completion signal, and read data from the RAM indicated by the fetch instruction.

98. The processing core according to any one of claims 65-87, wherein, at a same instant, the processing unit and the DMAC access different RAMs.

109. The processing core according to claim 78, wherein, at the same instant, the processing unit and the DMAC access different RAMs, comprising:
the at least two RAMs include a first RAM and a second RAM;
at a first timing, the processing unit reads first data from the first RAM, and the DMAC writes second data retrieved from the storage unit into the second RAM; and
at a second timing, the processing unit reads the second data from the second RAM, and the DMAC writes third data retrieved from the storage unit into the first RAM.