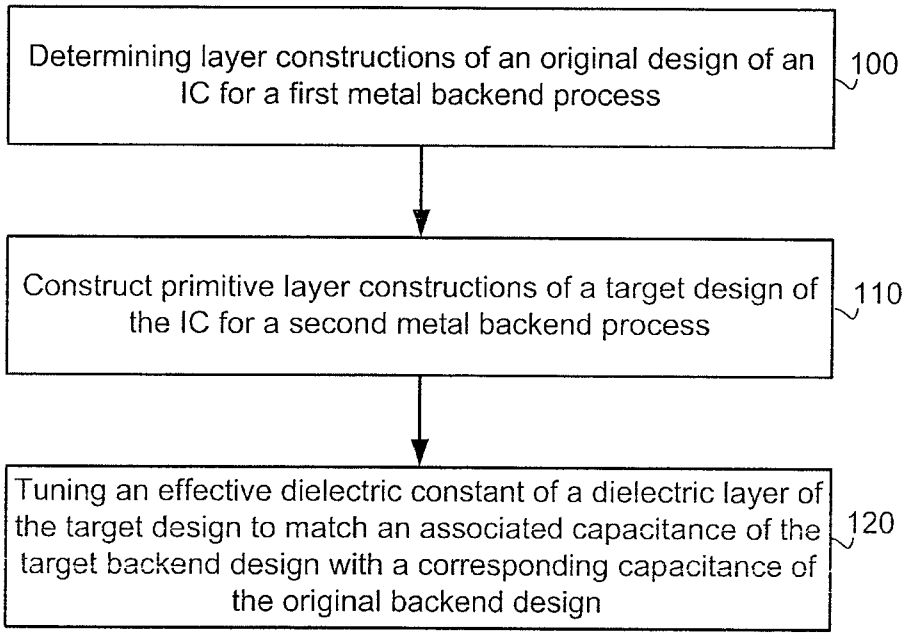

Determining layer constructions of an original design of an IC for a first metal backend process
100
Construct primitive layer constructions of a target design of the IC for a second metal backend process
110
Tuning an effective dielectric constant of a dielectric layer of the target design to match an associated capacitance of the target backend design with a corresponding capacitance of the original backend design
120

FIG. 1

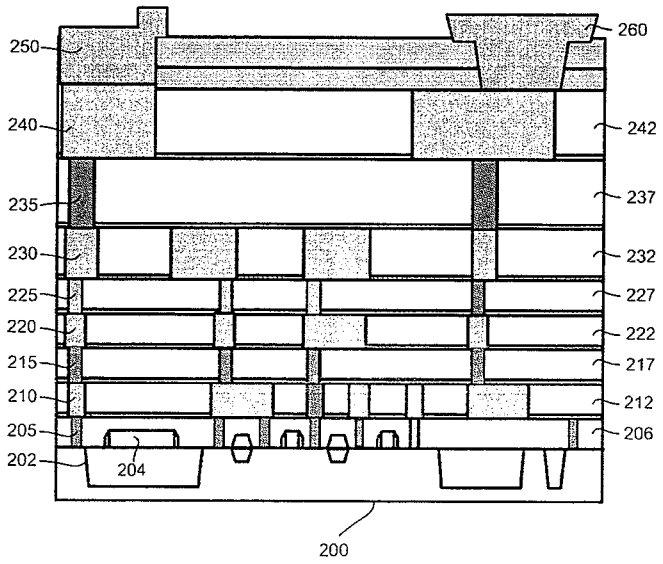

250
240
235
230
225
220
215
210
205
202
204
200
260
242
237
232
227
222
217
212
206

FIG. 2

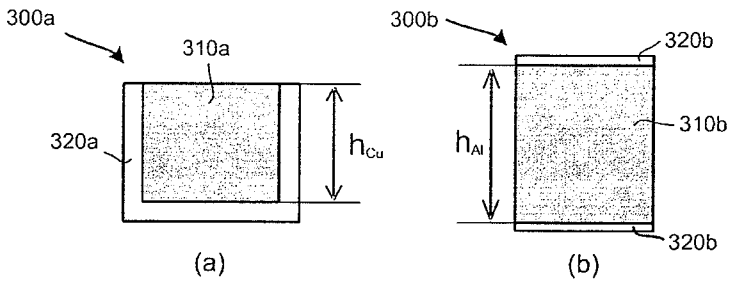

300a
310a
320a
h_{Cu}
(a)
300b
320b
310b
h_{Al}
320b
(b)

FIG. 3

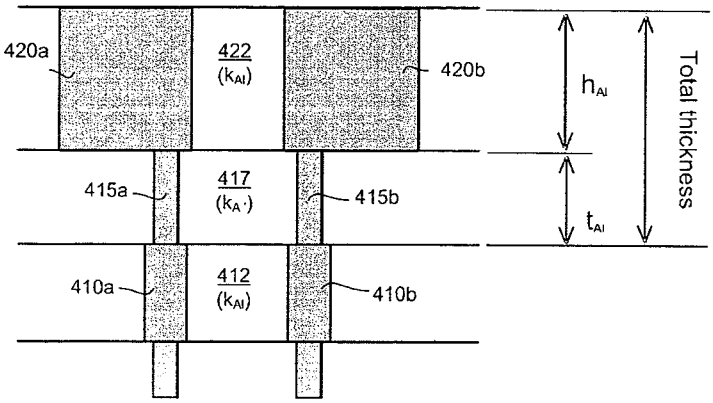

420a
422
(k_{Al})
420b
h_{Al}
Total thickness
415a
417
($k_{A\cdot}$)
415b
t_{Al}
410a
412
(k_{Al})
410b

FIG. 4

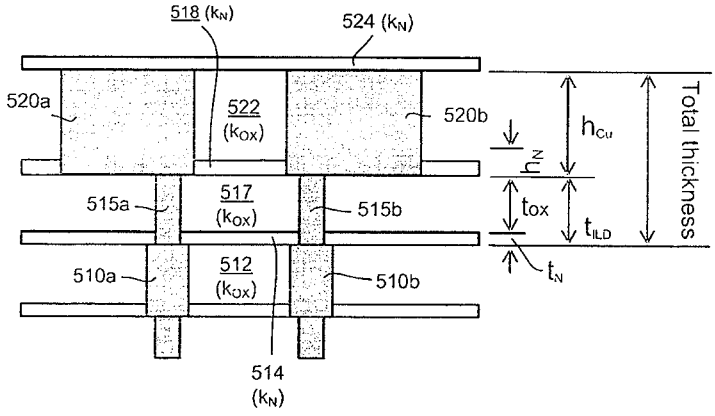

518 (k_N)
524 (k_N)
520a
522
(k_{OX})
520b
h_{Cu}
t_N
Total thickness
515a
517
(k_{OX})
515b
tox
t_{ILD}
510a
512
(k_{OX})
510b
t_N
514
(k_N)

FIG. 5

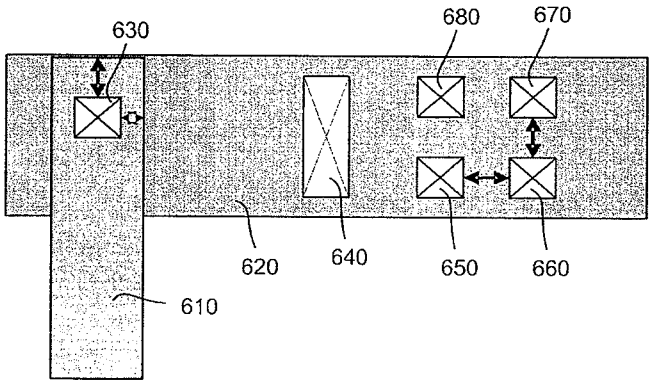


FIG. 6

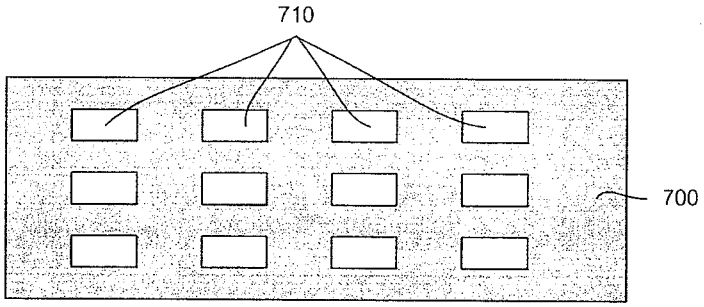


FIG. 7

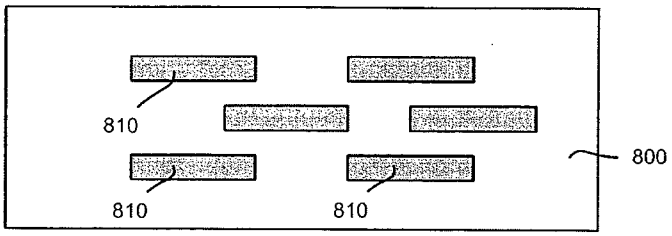

810
810
810
800

FIG. 8

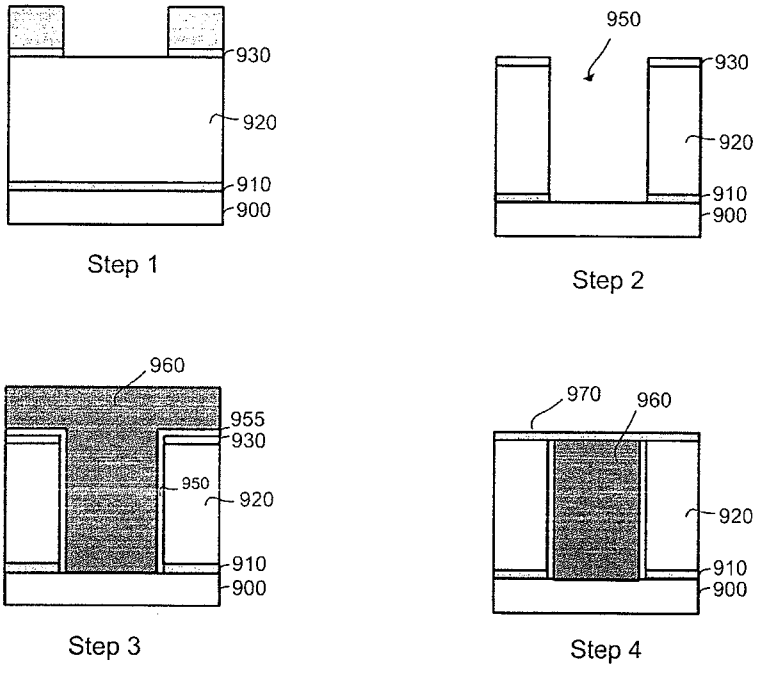
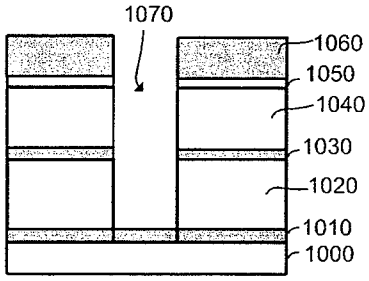
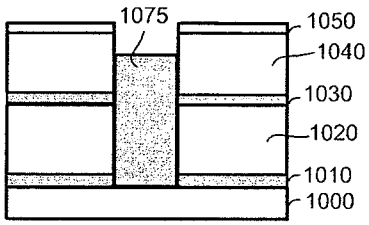

930
920
910
900
Step 1
950
930
920
910
900
Step 2
960
955
930
950
920
910
900
Step 3
970
960
920
910
900
Step 4

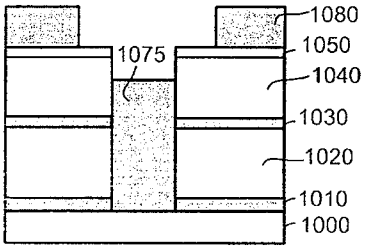
FIG. 9



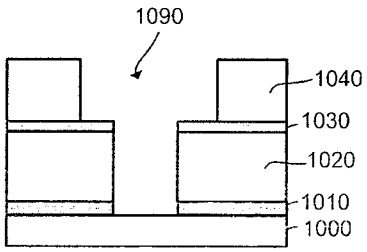
Step 1



Step 2



Step 3



Step 4

FIG. 10

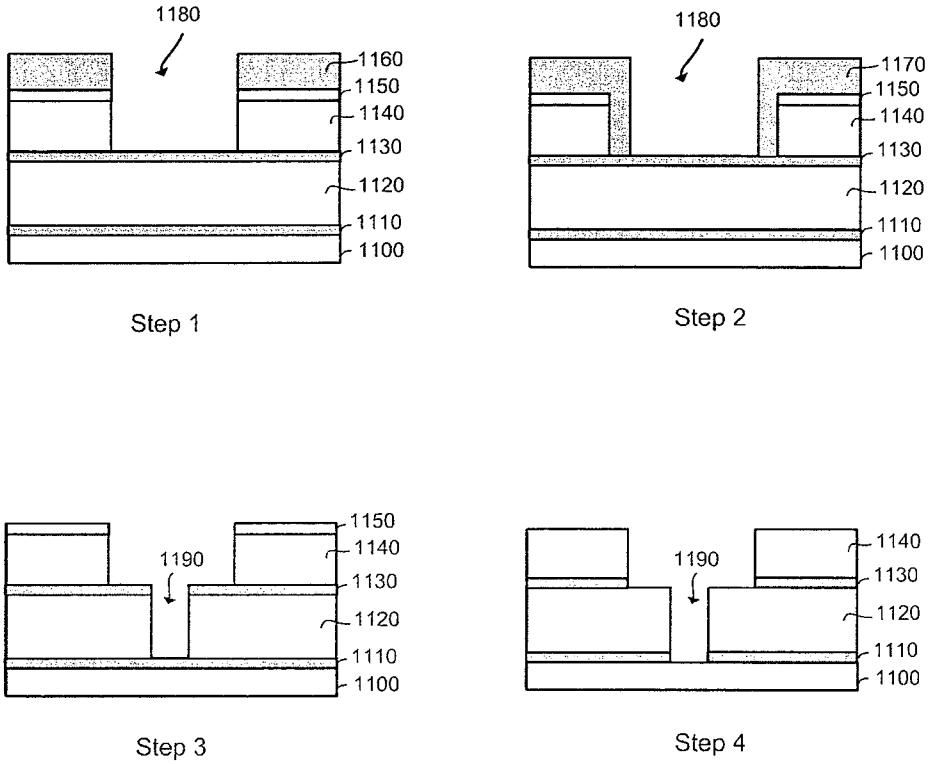

1180
1160
1150
1140
1130
1120
1110
1100
Step 1
1180
1170
1150
1140
1130
1120
1110
1100
Step 2
1190
1150
1140
1130
1120
1110
1100
Step 3
1190
1140
1130
1120
1110
1100
Step 4

FIG. 11

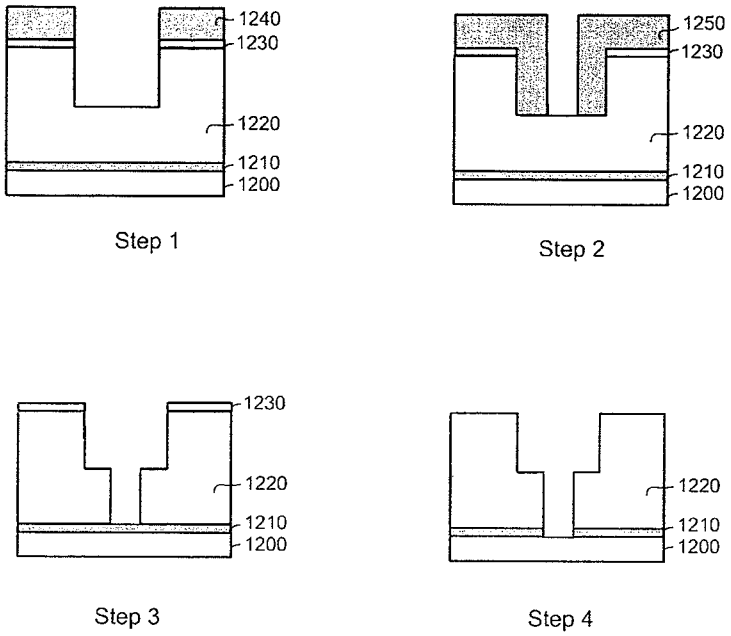

1240
1230
1220
1210
1200
Step 1
1250
1230
1220
1210
1200
Step 2
1230
1220
1210
1200
Step 3
1220
1210
1200
Step 4

FIG. 12