

METHOD AND SYSTEM FOR OPTIMIZING INTRA-FIELD CRITICAL DIMENSION UNIFORMITY USING A SACRIFICIAL TWIN MASK

ABSTRACT

Disclosed is a method and a system for optimizing intra-field critical dimension of an integrated circuit. A first mask for an integrated circuit is provided comprising at least one device region. A second mask is provided by copying the first mask and a lithography operation is provided to the integrated circuit using the first and second masks, wherein the critical dimension of the integrated circuit is optimized using the second mask. The second mask comprises a plurality of sacrificial patterns, which may be a plurality of flat patterns or a plurality of grating patterns.

Figure 1