



- (51) International Patent Classification:
H01L 35/32 (2006.01) *H01L 23/38* (2006.01)
- (21) International Application Number:
PCT/EP2015/001109
- (22) International Filing Date:
1 June 2015 (01.06.2015)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
PCT/EP2014/061335 2 June 2014 (02.06.2014) EP
- (72) Inventor; and
(71) Applicant : KILIC, Halil [TR/NL]; Troelstrakade 17,
NL-2531 AA Den Haag (NL).
- (74) Agent: DEMSKI, Siegfried; Patentanwälte Demski &
Nobbe, Tonhallenstr. 16, 47051 Duisburg (DE).
- (81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,

DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,
TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments (Rule 48.2(h))

(54) Title: INTEGRATED CIRCUIT WITH COOLING ARRAY

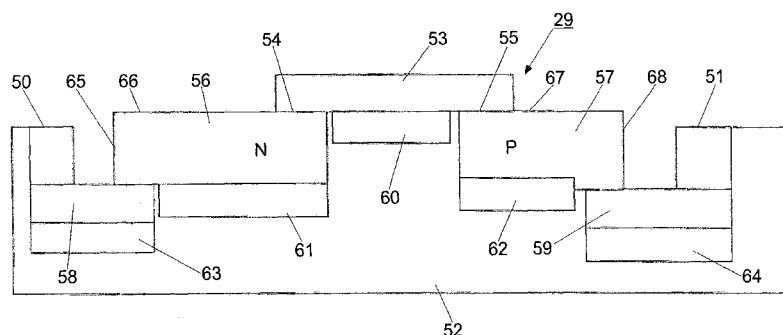


Fig. 5

(57) Abstract: The invention relates to an integrated circuit cooling array, preferably for a microprocessor or cooling apparatus, consisting of a dielectric substrate with doped and distinguished areas for the realization of at least one microelectronic component forming an integrated circuit, and at least one thermoelectric component forming a cooling array. The cooling array is characterized in that the thermoelectric component 1 comprises at least one first contact area, at least one second contact area and at least one cooling section whereat the cooling section is arranged between the first and the second contact area and consists of at least one thermal element 29, which is supplied with voltage by the first contact area and the second contact area through a control unit, whereat the thermal element 29 consists of at least one doped layer and a second doped layer, which are in such a way connected by a bridge element 53, 58, 59, 73, 83, 84, 92 that the bridge element 53, 58, 59, 73, 83, 84, 92 rests only partially on the first doped layer and/or the second doped layer. By means of the cooling array according to the invention compact and/or more efficient integrated circuits may be realized, since a sufficiently free heat flow from the inside of the integrated circuit is guaranteed.

