

ESD PROTECTION FOR HIGH DENSITY DRAMS
USING TRIPLE-WELL TECHNOLOGY

ABSTRACT OF THE DISCLOSURE

An ESD protected semiconductor circuit and the ESD protection circuit. The protected circuit includes a terminal (33), a semiconductor device (31) coupled to the terminal and an ESD protection circuit (35). The ESD protection circuit includes a substrate (1) of a first conductivity type and has a surface (9). A first well (3) of conductivity type opposite to the first conductivity type is disposed within the substrate and extends to the surface. A second well (5) of the first conductivity type is disposed within the first well and is spaced from the substrate and extending to the surface. A third region (7) of the opposite conductivity type is disposed within the second well and is spaced from the first well and extending to the surface. At least one of the substrate or the third region is coupled to the terminal.

Figure 1