METHOD OF CONTROLLING WELL LEAKAGE FOR TRENCH ISOLATIONS OF DIFFERING DEPTHS

TECHNICAL FIELD

This invention is generally directed to the field of semiconductor processing, and, more particularly, to a method of controlling well leakage in semiconductor devices having trench isolations of differing depths.

BACKGROUND ART

Modern integrated circuit devices are comprised of millions of semiconductor devices, *e.g.*, transistors, formed above a semiconducting substrate, such as silicon. These devices are very densely packed, *i.e.*, there is little space between them. These devices, or groups of devices, must be electrically isolated from other devices for the devices to perform their intended functions. Moreover, if the devices are not properly isolated, a variety of malfunctions may occur, *e.g.*, short circuit paths may be established, etc.

To insure that devices, or groups of devices, are properly isolated, modern semiconductor processing involves the formation of shallow trench isolations (STI) in various regions of the substrate. These shallow trench isolations are typically formed by etching a trench in the semiconductor substrate and, thereafter, filling the trench with an isolation material, *e.g.*, an insulator, such as silicon dioxide, silicon oxynitride, silicon nitride, or other like materials.

After the trench isolations are formed, an ion implantation process is typically performed to implant dopant atoms through the trench isolations and into the substrate beneath the trench isolations. The purpose of this implant process, sometimes referred to as the "channel-stop" implant, is to help insure that the semiconductor device is properly isolated. In short, this implant helps to prevent the unwanted migration of electrons beyond certain defined boundaries. The type of dopant atoms used, as well as the various energy levels used in the ion implantation process, will vary depending upon the device under construction. For example, for NMOS devices, the channel-stop implant may be comprised of a P-type dopant material, such as boron. For PMOS devices, the channel-stop implant may be comprised of an N-type dopant material, such as arsenic or phosphorous.

It is intended that the implantation process is performed in such a manner that the peak concentration of the channel-stop implant is at or slightly below the bottom of the trench isolation. Of course, subsequent heat treatment processes may cause the dopant atoms to migrate to some degree. The parameters of the implant process used to form the channel-stop implant is based upon an assumed trench depth and/or thickness of the isolation material through which the channel-stop implant will be performed. However, a variety of manufacturing variations may adversely impact the formation of acceptable, or at least more effective, channel-stop implants.

For example, the trench depth, as formed, may be greater or less than anticipated, due to operator error, variations within the etching tool used to form the trench, etc. Additionally, the thickness of the isolation material formed in the trench through which the channel-stop implant process will be performed may be thicker or thinner than anticipated due to errors in polishing or in forming the isolation material, etc.

The variations, if not accounted for, may lead to the formation of less effective channel-stop implants, and, thus, less effective isolation of semiconductor devices. For example, if the trench is formed deeper than anticipated and/or the thickness of the isolation material in the trench is greater than anticipated, performing a channel-stop implant process based upon assumed design parameters for the trench depth and thickness of the isolation material will result in an implant that does not penetrate into the substrate as deeply as would otherwise be desired. Conversely, if the trench is formed too shallow and/or the thickness of the isolation material is less than

anticipated, the resulting channel-stop implant may be formed deeper in the substrate than would otherwise be desired. Moreover, proper formation of channel-stop implants becomes even more important in modern semiconductor fabrication where the width of the trench isolation is reduced as integrated circuit devices become more densely packed.

The present invention is directed to a method of forming a semiconductor device that minimizes or reduces some or all of the aforementioned problems.

DISCLOSURE OF INVENTION

The present invention is directed to a method of controlling well leakage for trench isolations of differing depths. In one embodiment, the method comprises forming a trench in a semiconducting substrate and forming an isolation material in the trench. The method further comprises determining at least one of the depth of the trench and the thickness of the trench isolation material and determining an energy level for an ion implantation process to be performed through the isolation material based upon at least one of the determined depth of the trench and the determined thickness of the isolation material.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 is a cross-sectional view of an illustrative prior art semiconductor device formed above a semiconducting substrate;

Figure 2 is an enlarged cross-sectional view of one illustrative embodiment of a trench isolation structure;

Figure 3 is a flowchart depicting one illustrative embodiment of the present invention; and

Figure 4 depicts an illustrative embodiment of a system that may be used with the present invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

MODE(S) FOR CARRYING OUT THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present invention will now be described with reference to Figures 1-4. Although the various regions and structures of a semiconductor device are depicted in the drawings as having very precise, sharp configurations and profiles, those skilled in the art recognize that, in reality, these regions and structures are not as precise as indicated in the drawings. Additionally, the relative sizes of the various features depicted in the drawings may be exaggerated or reduced as compared to the size of those feature sizes on fabricated devices. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present invention.

In general, the present invention is directed to a method of controlling well leakage for trench isolations of differing depths. As will be readily apparent to those skilled in the art upon a complete reading of the present application, the present method is applicable to a variety of technologies, *e.g.*, NMOS, PMOS, CMOS, etc., is readily applicable to a variety of devices, including, but not limited to, logic devices, memory devices, etc.

As shown in Figure 1, an illustrative semiconductor device 12 is formed above a surface 11 of a semiconducting substrate 10. The device 12 is formed within an active area 13 in the substrate 10 that is defined by the trench isolation 21. The illustrative semiconductor device 12 depicted in Figure 1 is an NMOS transistor comprised of a gate insulation layer 16, a gate electrode 14, sidewall spacers 20 and source/drain regions 18. The various components of the illustrative transistor depicted in Figure 1 may be formed by a variety of techniques, and they may be comprised of a variety of different materials. Thus, neither the particular technique used to form the illustrative semiconductor device 12, nor the materials or construction of the device 12, should not be considered a limitation of the present invention.

Initially, trench isolations 21 are formed in the substrate 10. Figure 2 is an enlarged cross-sectional view of an illustrative trench isolation 21. In particular, a trench 22 is formed in the substrate 10 by an etching process, such as an anisotropic etching process. The trench 22 has a bottom 28 that defines the depth of the trench 22. The width, depth and shape of the trench 22 may vary depending upon the device under construction. Thus, the particular configuration, width and depth of the trench 22 depicted herein should not be considered a limitation of the present invention unless it is specifically set forth in the appended claims.

Thereafter, an isolation material 24 is formed in the trench 22. This may be accomplished by a variety of techniques, *e.g.*, depositing or growing a layer of material across the entire surface 11 of the substrate 10 and in the trench 22. The trench isolation material 24 may be comprised of a variety of materials that are suitable to perform the function of isolating the semiconductor device, *e.g.*, an oxide, an oxynitride, a nitride, silicon dioxide, silicon oxynitride, silicon nitride, etc. Thereafter, a chemical mechanical polishing operation may be performed to planarize a surface 23 of the trench isolation material 24 such that it is substantially planar with the surface 11 of the substrate 10. Alternatively, a planarization operation may be performed such that the surface 23 of the isolation material 24 is approximately planar with the surface of another process layer (not shown) that was previously formed above the surface of the substrate 10. In the depicted embodiment, the isolation material 24 has a top surface 23 that is approximately planar with the surface 11 of the substrate 10. Of course, as will be recognized by those skilled in the art, the top surface 23 of the isolation material 24 may extend above the surface 11 of the substrate 10 when the formation of the trench isolation 21 is complete.

After the isolation material 24 is formed in the trench 22, an ion implantation process, as indicated by arrows 30, is used to form schematically depicted channel-stop implants 26, as shown in Figure 2. A masking layer 31, *e.g.*, photoresist, is formed on the substrate 10 and patterned to expose the trench isolation 21 to the ion implantation process 30. The dopant atoms used to form the channel-stop implant 26 will vary, depending upon the type of device under construction, boron, phosphorous, arsenic, etc.

As stated previously, the depth of the implant and, in particular, the depth of the peak concentration of the channel-stop implant, will vary, depending upon the depth of the trench 22 and the thickness of the isolation material 24 through which the ion implantation process will be performed to form the channel-stop implant. However, to insure that the channel-stop implant 26 is more precisely positioned, variations in the trench depth and/or the thickness of the isolation material 24 are determined, and that information is used to vary the energy level of the ion implantation process used to form the channel-stop implants 26. In effect, the information

regarding the depth of the trench 22 and/or the thickness of the isolation material 24 may be fed-forward and used to vary the energy level of the ion implantation process used to form the channel-stop implants 26. This may be done on a lot-by-lot basis or on a wafer-by-wafer basis.

For example, if it is determined that the trench 22 is deeper than anticipated, or that the isolation material 24 is thicker than anticipated, then the energy level for the ion implantation process may be increased relative to what it would have otherwise been had the depth of the trench 22 and/or the thickness of the isolation material 24 been as anticipated. Conversely, if it is determined that the trench 22 is shallower than anticipated, or that the isolation material 24 is thinner than anticipated, the energy level of the ion implantation process may be reduced.

Figure 3 depicts one illustrative embodiment of the present invention in flowchart form. As shown therein, the method of the present invention comprises forming a trench 22 in a semiconducting substrate, as indicated at block 32, and forming an isolation material 24 in the trench 22, as indicated at block 34. The method further comprises determining at least one of the depth of the trench 22 and the thickness of the isolation material 24, as indicated at block 36, and determining an implant energy for an ion implantation process to be performed through the isolation material based upon at least one of the determined depth of the trench 22 and the thickness of the isolation material 24.

As set forth previously, the step of forming the trench 22, as indicated at block 32, may be performed by a variety of processes, *e.g.*, an anisotropic etching process. Moreover, the resulting trench 22 may take any shape, and it may have very low or high aspect ratios. Forming the trench isolation material 24, as indicated at block 34, may also be accomplished by a variety of techniques, *e.g.*, deposition, thermal growth, etc. Moreover, the trench isolation material 24 may be comprised of a variety of materials, *e.g.*, an oxide, an oxynitride, etc.

With respect to determining the depth of the trench 22, as indicated at block 36, this may be accomplished by measuring the depth of the trench 22 using a metrology tool, such as an alpha step system tool. With respect to the illustrative embodiment of the trench 22 depicted in Figure 2, the depth of the trench 22 would be considered to be the approximate distance between the surface 11 of the substrate 10 and the bottom surface 28 of the trench 22. The thickness of the isolation material 24 may also be determined, as indicated at block 36, using a metrology tool, such as an ellipsometer, a Thermawave tool. The thickness of interest with respect to the isolation material 24 would be the amount of isolation material through which the channel-stop ion implantation process would be performed to form the channel-stop implants 26. In the illustrative embodiment depicted in Figure 2, the thickness dimension of interest would be the dimension from the surface 23 of the isolation material 24 to the bottom surface 28 of the trench 22. Measuring the depth of the trench 22 and/or the thickness of the isolation material 24 may be done on a representative basis, *i.e.*, sufficient measurements may be made to satisfy the user as to the accuracy of the measurements. The measurements may be used for subsequent processing of wafers on a lot-by-lot basis or on a wafer-by-wafer basis.

Determining an implant energy for the channel-stop ion implantation process, as indicated at block 38, may be accomplished by a variety of techniques. For example, a database may be developed that correlates the determined depth of the trench 22 and/or the determined thickness of the isolation material 24 to a corresponding energy level for the channel-stop implantation process. Alternatively, the energy level could be calculated based upon the determined depth off the trench 22 and/or the thickness of the isolation material 24. Other methodologies are also possible. Thereafter, the method continues with performing the ion implantation process through the isolation material 24 at the determined energy level.

In one embodiment of the present invention, the energy level of the channel-stop implantation process varies or is adjusted, depending upon the depth of the trench 22 and/or the thickness of the isolation material 24. One illustrative system that may be used in accordance with the present invention is depicted in Figure 4. As shown therein, a system 50 for processing wafers 52 is comprised of a metrology tool 44, an automatic process controller 48, and an ion implantation tool 46. The metrology tool 44 is used to measure the depth of the trench 22 and/or the thickness of the isolation material 24. The metrology tool 44 may be any type of device capable of performing the desired measurements.

In one embodiment, the automatic process controller 48 interfaces with the metrology tool 44 and the ion implantation tool 46. The controller 48 may be used to determine or control the energy level of the ion implantation process performed in the ion implantation tool 46, depending upon the depth of the trench 22 and/or the thickness of the isolation material 24, as determined by the metrology tool 44. That is, the depth of the trench 22 and/or the thickness of the isolation material 24 is fed-forward to the controller 48, and the energy level of the channel-stop implant process performed in the ion implant tool 46 is controlled based upon at least one of those parameters. The controller 48 may be a stand-alone device, it may be part of a system, or it may be part of the ion implant tool 46 or another process tool, such as a chemical mechanical polishing tool. Moreover, the metrology tool 44 may be a stand-alone device or system, or it may be incorporated into the ion implant tool 46, another processing tool, *e.g.*, a chemical mechanical polishing tool, an etch tool, etc., or a system containing both.

In the illustrated embodiment, the automatic process controller 48 is a computer programmed with software to implement the functions described. However, as will be appreciated by those of ordinary skill in the art, a hardware controller (not shown) designed to implement the particular functions may also be used. Portions of the invention and corresponding detailed description are presented in terms of software, or algorithms and symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the ones by which those of ordinary skill in the art effectively convey the substance of their work to others of ordinary skill in the art. An algorithm, as the term is used here, and as it is used generally, is conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of optical, electrical, or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise, or as is apparent from the discussion, terms such as "processing" or "computing" or "calculating" or "determining" or "displaying" or the like, refer to the actions and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical, electronic quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

An exemplary software system capable of being adapted to perform the functions of the automatic process controller 48, as described, is the ObjectSpace Catalyst system offered by ObjectSpace, Inc. The ObjectSpace Catalyst system uses Semiconductor Equipment and Materials International (SEMI) Computer Integrated Manufacturing (CIM) Framework compliant system technologies, and is based on the Advanced Process Control

(APC) Framework. CIM (SEMI E81-0699 - Provisional Specification for CIM Framework Domain Architecture) and APC (SEMI E93-0999 - Provisional Specification for CIM Framework Advanced Process Control Component) specifications are publicly available from SEMI.

Through use of the present invention, effective trench isolations may be made while accounting for variations in trench depth and/or the thickness of the isolation material. As a result, more effective trench isolations may be manufactured and used in modern semiconductor devices.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

1. A method comprising:

forming a trench (22) in a semiconducting substrate (10), said trench having a depth;

forming an isolation material (24) in said trench (22), said isolation material (24) having a thickness;

determining at least one of the depth of said trench (22) and the thickness of said isolation material (24); and

determining an energy level for an ion implantation process to be performed through said isolation material (24) based upon at least one of said determined depth of said trench (22) and said thickness of said isolation material (24).

2. The method of claim 1, wherein forming a trench (22) in a semiconducting substrate (10) comprises etching a trench (22) in a semiconducting substrate.

3. The method of claim 1, wherein forming a trench isolation material (24) in said trench (22) comprises forming a trench isolation material (24) comprised of at least one of an oxide, an oxynitride, and a nitride in said trench (22).

4. The method of claim 1, wherein determining at least one of the depth of said trench (22) and the thickness of said isolation material (24) comprises measuring at least one of the depth of said trench (22) and the thickness of said isolation material (24).

5. The method of claim 1, wherein determining an energy level for an ion implantation process to be performed through said isolation material (24) based upon at least one of said determined depth of said trench (22) and said thickness of said isolation material (24) comprises calculating an energy level for an ion implantation process to be performed through said isolation material (24) based upon at least one of said determined depth of said trench (22) and said thickness of said isolation material (24).

6. The method of claim 1, wherein determining an energy level for an ion implantation process to be performed through said isolation material (24) based upon at least one of said determined depth of said trench (22) and said thickness of said isolation material (24) comprises correlating an energy level for an ion implantation process to be performed through said isolation material (24) with at least one of said determined depth of said trench (22) and said thickness of said isolation material (24).

7. The method of claim 1, further comprising reporting said at least one of said determined depth of said trench and said thickness of said isolation material to a controller that controls the implant energy of an ion implantation tool used to perform an ion implantation process through the isolation material.

8. The method of claim 1, further comprising performing the ion implantation process using the determined energy level.

9. A system comprising:

a metrology tool (44) for determining at least one of a depth of a trench (22) and a thickness of an isolation material (24) formed in said trench;

a controller (48) for determining an energy level for an ion implantation process to be performed through said isolation material (24) based upon at least one of the determined depth and thickness; and

an ion implant tool (46) for performing said ion implantation process at said determined energy level.