Claims

What is claimed is:

1. A method for fabricating a semiconductor device, comprising:

forming a magnetic tunneling junction (MTJ) stack on a substrate;

forming a top electrode on the MTJ stack;

forming an etch stop layer on the top electrode;

forming a first spin orbit torque (SOT) layer on the etch stop layer; and

patterning the first SOT layer, the etch stop layer, the top electrode and the MTJ stack to form a MTJ.

2. The method of claim 1, wherein the substrate comprises a magnetic random access memory (MRAM) region and a logic region, the method comprising:

forming a first inter-metal dielectric (IMD) layer on the substrate;

forming a first metal interconnection in the first IMD layer on the MRAM region;

forming a hard mask on the first SOT layer;

forming the MTJ on the first metal interconnection;

forming a cap layer on the hard mask and the first IMD layer;

forming a second IMD layer on the cap layer;

forming a second SOT layer on the hard mask and the second IMD layer;

patterning the second SOT layer;

forming a third IMD layer on the second SOT layer; and

forming a second metal interconnection on the logic region.

3. The method of claim 2, further comprising:

patterning the cap layer;

forming the second IMD layer on the cap layer;

removing the cap layer and the second IMD layer to expose the hard mask, wherein a top surface of the cap layer is lower than a top surface of the first SOT layer; and

forming the second SOT layer on the hard mask, the cap layer, and the second IMD layer.

4. The method of claim 3, further comprising patterning the cap layer and the first IMD layer, wherein a sidewall of the cap layer is aligned with a sidewall of the first IMD layer.

5. The method of claim 2, further comprising:

removing the cap layer to form a spacer around the MTJ, the etch stop layer, and the first SOT layer;

forming the second IMD layer on the spacer;

planarizing the second IMD layer;

forming the second SOT layer on the hard mask and the second IMD layer;

patterning the second SOT layer;

forming the third IMD layer on the second SOT layer; and

forming the second metal interconnection on the logic region.

6. The method of claim 2, further comprising:

forming a stop layer on the third IMD layer;

forming a fourth IMD layer on the stop layer;

forming a third metal interconnection on the MRAM region to connect to the second SOT layer; and

forming a fourth metal interconnection on the logic region to connect to the second metal interconnection.

7. A semiconductor device, comprising:

a magnetic tunneling junction (MTJ) on a substrate;

a top electrode on the MTJ;

a first spin orbit torque (SOT) layer on the top electrode;

an etch stop layer between the top electrode and the first SOT layer; and

a second SOT layer on the first SOT layer.

8. The semiconductor device of claim 7, wherein the substrate comprises a magnetic random access memory (MRAM) region and a logic region, the semiconductor device comprising:

a first inter-metal dielectric (IMD) layer on the substrate;

a first metal interconnection in the first IMD layer on the MRAM region;

the MTJ on the first metal interconnection;

a second IMD layer around the MTJ; and

a second metal interconnection in the second IMD layer on the logic region.

9. The semiconductor device of claim 8, further comprising:

a stop layer on the second IMD layer;

a third IMD layer on the stop layer;

a third metal interconnection on the MRAM region to connect to the second SOT layer; and

a fourth metal interconnection on the logic region to connect to the second metal interconnection.

10. The semiconductor device of claim 7, further comprising a hard mask between the first SOT layer and the second SOT layer.

11. The semiconductor device of claim 7, further comprising a spacer adjacent to the MTJ and the first SOT layer.

12. The semiconductor device of claim 11, wherein the spacer comprises a L-shape.

13. The semiconductor device of claim 12, wherein a top surface of the spacer is lower than a top surface of the first SOT layer.

14. The semiconductor device of claim 11, wherein the spacer comprises an I-shape.

15. The semiconductor device of claim 14, wherein top surfaces of the spacer and the first SOT layer are coplanar.