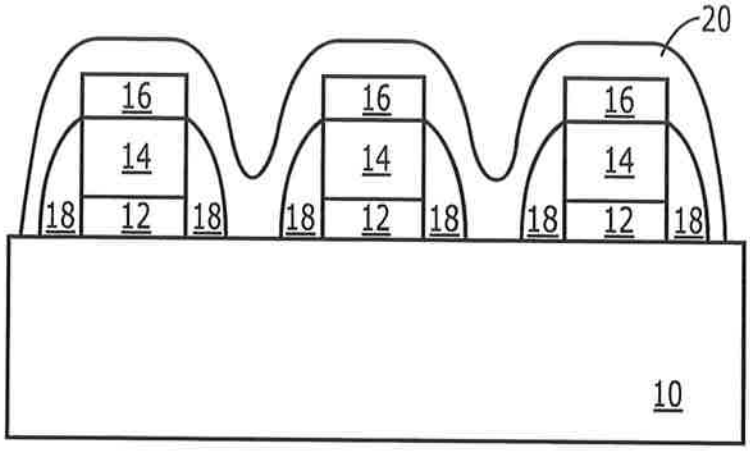

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FIG. 1A

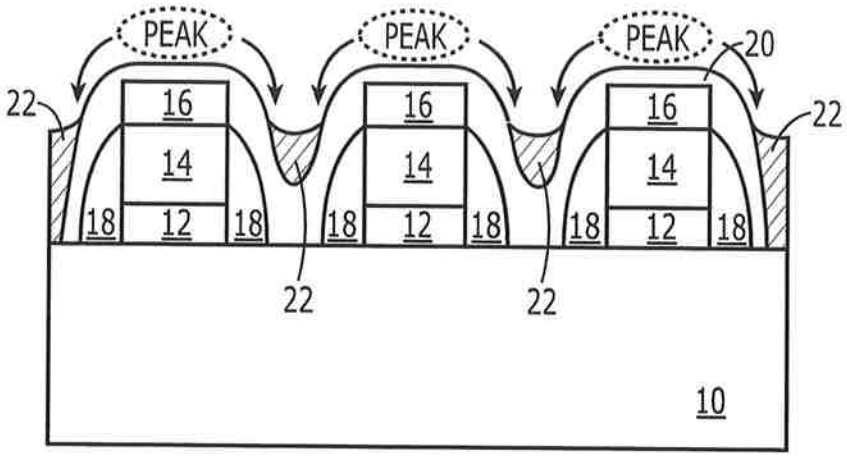

PEAK
PEAK
PEAK
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FIG. 1B

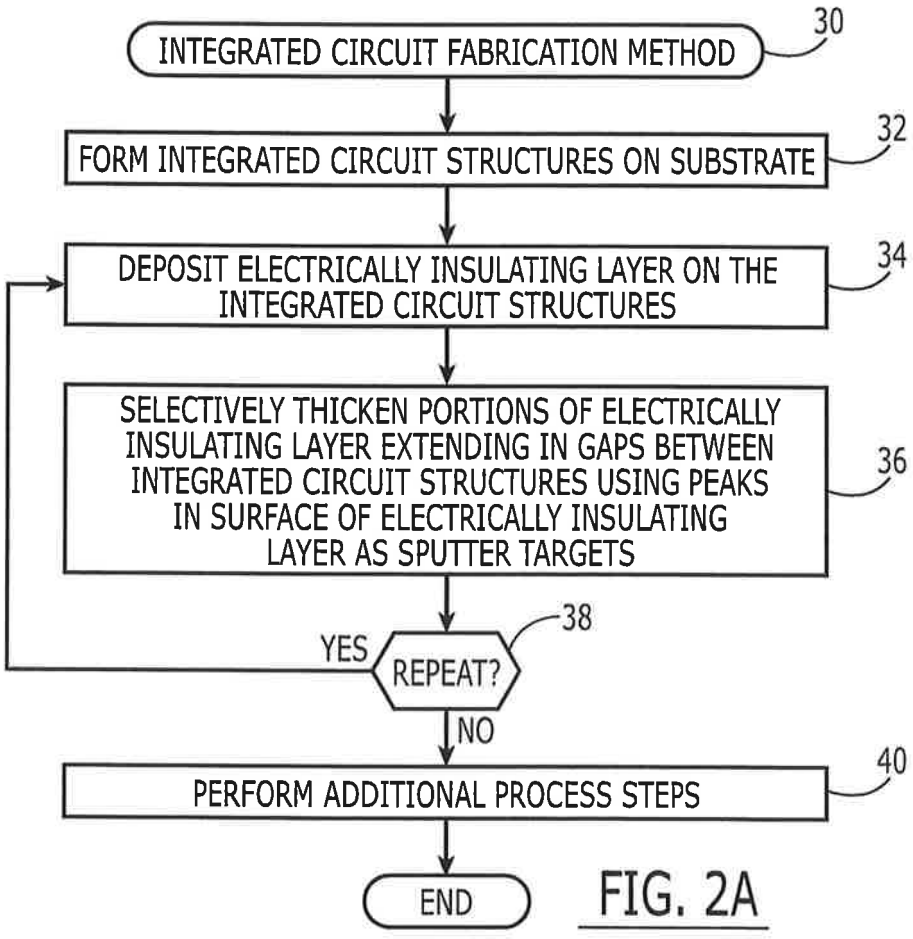

INTEGRATED CIRCUIT FABRICATION METHOD
30
FORM INTEGRATED CIRCUIT STRUCTURES ON SUBSTRATE
32
DEPOSIT ELECTRICALLY INSULATING LAYER ON THE INTEGRATED CIRCUIT STRUCTURES
34
SELECTIVELY THICKEN PORTIONS OF ELECTRICALLY INSULATING LAYER EXTENDING IN GAPS BETWEEN INTEGRATED CIRCUIT STRUCTURES USING PEAKS IN SURFACE OF ELECTRICALLY INSULATING LAYER AS SPUTTER TARGETS
36
YES
REPEAT?
38
NO
PERFORM ADDITIONAL PROCESS STEPS
40
END

FIG. 2A

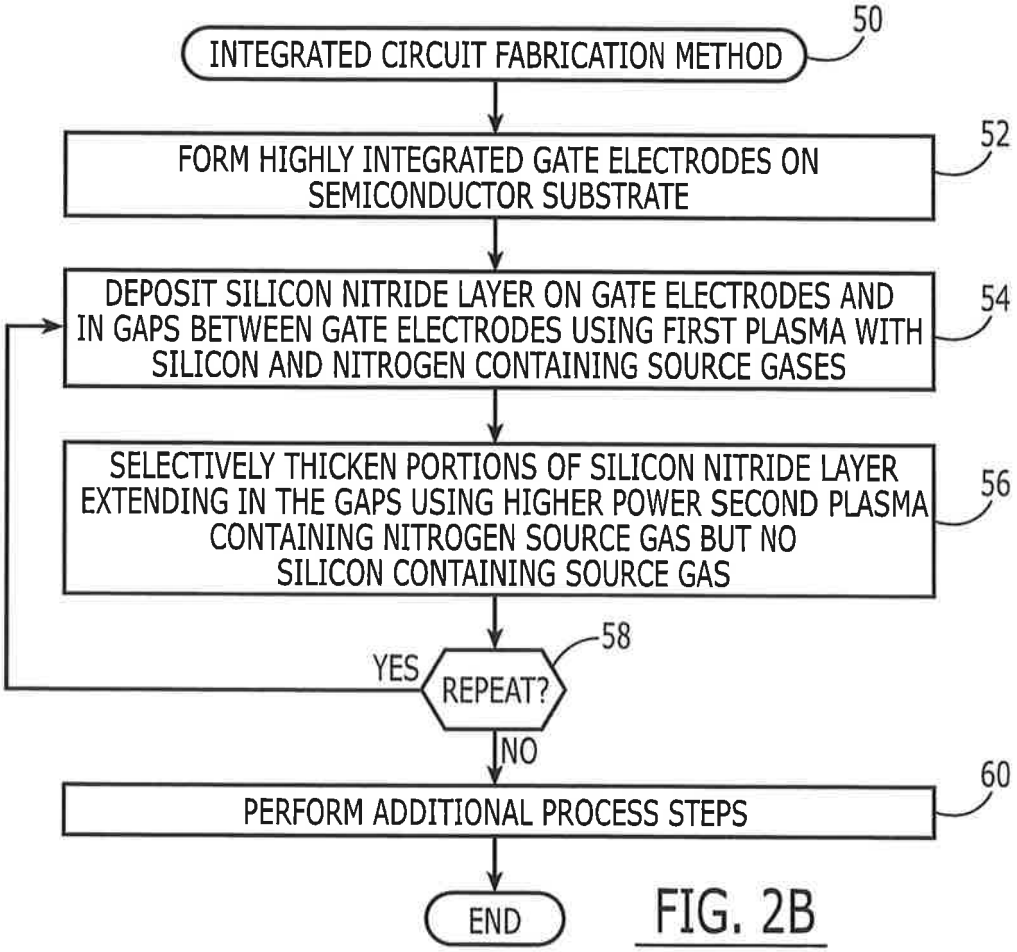

INTEGRATED CIRCUIT FABRICATION METHOD
50
FORM HIGHLY INTEGRATED GATE ELECTRODES ON SEMICONDUCTOR SUBSTRATE
52
DEPOSIT SILICON NITRIDE LAYER ON GATE ELECTRODES AND IN GAPS BETWEEN GATE ELECTRODES USING FIRST PLASMA WITH SILICON AND NITROGEN CONTAINING SOURCE GASES
54
SELECTIVELY THICKEN PORTIONS OF SILICON NITRIDE LAYER EXTENDING IN THE GAPS USING HIGHER POWER SECOND PLASMA CONTAINING NITROGEN SOURCE GAS BUT NO SILICON CONTAINING SOURCE GAS
56
YES
REPEAT?
58
NO
PERFORM ADDITIONAL PROCESS STEPS
60
END

FIG. 2B