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(54) Title: SELF-ALIGNED TOP VIA

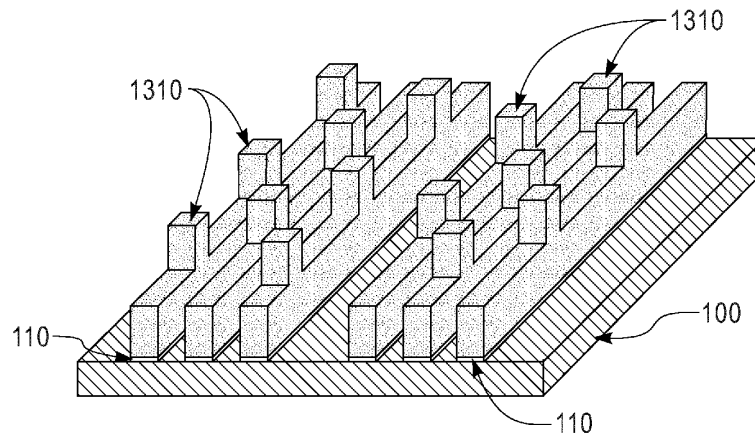


FIG. 16

(57) Abstract: SELF-ALIGNED TOP VIAEmbodiments of the invention include a method for fabricating a semiconductor device and the resulting structure. Mandrels are patterned on a liner, where the liner is located on a semiconductor substrate. Spacers are formed on sidewalls of the mandrels. Dielectric material lines are formed on exposed surfaces of the liner and within a plurality of gaps between the spacers. The mandrels are removed. The at least one of the dielectric material lines are removed from within at least one of the plurality of gaps between the spacers. Conductive metal is formed within each gap. The conductive metal is patterned to form metal interconnect lines and vias. The plurality of spacers and the remaining dielectric material lines are removed.

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