FACE-TO-FACE MULTI-CHIP PACKAGE

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a semiconductor packaging structure, and more particularly, to a face-to face multi-chip package.

Description of the Related Art

As the technology of semiconductor fabrication grows more and more advanced, the relevant techniques have to be further developed to coordinate the requirements of the semiconductor devices. The fabrication process of a semiconductor device typically includes three stages. In the first stage, an epitaxy technique is used for the formation of a semiconductor substrate. Semiconductor devices such as metal-oxide semiconductor (MOS) and multilevel interconnection are fabricated on the substrate in the second stage. The third stage is the packaging process. It is now a leading trend for fabricating a device or an electronic product with a thin, light, and small dimension, that is, with a higher integration for semiconductor devices. In terms of packages, many techniques such as chip scale package, multi-chip module (MCM) have been developed to obtain a high integration. The development of the fabrication technique with a line width of 0.18μm has evoked a great interest and intensive research to further decrease the package volume. It is thus one of the very important package techniques to arrange more than one chips into a single package. In

a multi-chip package, chips of processor, memory, including dynamic random access memory (DRAM) and flash memory, and logic circuit can be packed together in a single package to reduce the fabrication cost and the packaging volume. Furthermore, the signal transmission path is shortened to enhance the efficiency. The multi-chip IC packaging technology may also be applied to a multi-chip system with variable functions and operation frequencies, for example,

1. A system comprises memory chips, microprocessors, resistors, capacitors, and inductors.

2. A system comprises memory chips (DRAM), logic circuit chips, and memory chips (Flash memory),

3. A system comprises analog chips, logic circuit chips, memory chips (including DRAM, SRAM, Flash memory), resistor, capacitor, and inductor.

In Fig. 1, a conventional multi-chip module is shown. A multi-level printed circuit board (PCB) is typically applied as a substrate of the to the carrier of a multi-chip module. More than one chips 12 are adhered on the substrate 10 by insulation glue 14. The bonding pads on the chip 12 are electrically connected to the terminals on the substrate 10 by conductive wires 16. In addition to wire bonding, the connection between the chip 12 and the substrate 10 can also be established by flip chip or controlled collapse chip connection (C4) with the formation of a bump. A resin 18 is used to seal the chip 12, and the electrical connection between the whole package and a printed circuit board can be achieved by ball grid array (BGA) which use solder balls 20 to connect the terminals on the printed circuit board. The drawback of this conventional multi-chip module includes a large surface is occupied since chips are

packaged on a same side of surface. Therefore, the volume of the package is large, and the signal path between chips is long. In addition, though the volume of the package can be reduced by using flip chip technique to achieve the connection between the chip and the carrier, the connection between chips still has to be achieved by printed circuits on the substrate 10. Therefore, it is not possible to effectively reduce signal transmission path and to shrink the volume or surface area at once. A low yield and a high cost are thus resulted.

To further shrink the volume of package, a face to face multi-chip package is disclosed in US Patent no. 5,331,235. In Fig. 2, this multi-chip package comprises two chips 30 and 32 disposed face to face by way of tape automatic bonding (TAB). For the part of inner lead bonding (ILB), two chips 30, 32 having bumps 34, 36 to electrically connect the film carrier 38. In the part of outer lead bonding (OLB), the chips 30, 32 connect to a lead frame 40. A solder ball 42 is formed between the chips 30, 32. The chips 30, 32, the film carrier 38 and the lead frame 40 are then molded with resin 44. This multi-chip package uses tape automatic bonding technique. The electrical connection between chips and printed circuit board is achieved by the installation of a lead frame or other carriers. The signal transmission path is lengthened. In addition, a film carrier is used to achieve the connection between chips, the layout of metal pad on the chips is formed by a line layout or a peripheral layout. Thus, it can not meet the integration requirement for semiconductors with greatly increased number of input/output (I/O) nodes due to further highly integration.

SUMMARY OF THE INVENTION

The invention provides a face-to-face multi-chip package with a reduced thickness and surface area. More than one chip can be packaged on one carrier.

It is another object of the invention to provide a face-to-face multi-chip package. The multi-chip chip scale package has a shortened signal transmission path to enhance the performance of the chips.

Bonding pads are allocated on the chip with as an area array to increase the integration of the package. In addition, the rear sides of chips are bared, so that the heat dissipation is enhanced.

To achieve the above-mentioned objects and advantages, a face-to-face multi-chip package is provided. A flip-chip technique is employed. More than one chip are disposed face-to-face and electrically connected via bumps.

In another embodiment of the invention, an anisotropic conductive pasted is filled between the chips to improve the electrical connection. A flip chip technique is used, so that the pads can be distributed on the pads in an area array. Therefore, the integration is enhanced. A heat dissipation apparatus can be further installed on the other side of the chips to improve the performance of heat dissipation.

In addition, the face-to-face multi-chip package in the invention can use lead frame, film carrier, printed circuit board, or glass as a carrier. The package is applicable in many different types of packages such as ball grid array package, chips on board (COB), chips on glass (COG), and multi-chip chip scale package (MCCSP). An improved packaging quality and an enhanced reliability are obtained.

Both the foregoing general description and the following detailed description are

exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a conventional multi-chip module package;

Figure 2 is a cross sectional view showing a conventional face-to-face multi-chip module package;

Figure 3A and Figure 3B are cross sectional views showing a face-to-face multi-chip package in a first embodiment according to the invention;

Figure 3C and Figure 3D are cross sectional views showing the face-to-face multi-chip package in the first embodiment added with a heat dissipation apparatus;

Figure 4A is a cross sectional view showing a face-to-face multi-chip package in a second embodiment according to the invention;

Figure 4B to Figure 4C are cross sectional views showing the face-to-face multi-chip package in the second embodiment added with a heat dissipation apparatus;

Figure 5A and Figure 5B are cross sectional views showing a face-to-face multi-chip package in a third embodiment according to the invention; and

Figure 5C and Figure 5D are cross sectional views showing the face-to-face multi-chip package in the third embodiment added with a heat dissipation apparatus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

During the process of packages, several stages are typically included:

1) Selection of carriers: types of chips have to be selected according specific requirement, for example, lead frame, film carrier, or printed circuit board. The film

carriers are commonly used for the technique of tape automatic bonding (TAB);

2) Electrical connections between chips and carriers: currently, techniques such as wire bonding, film automatic bonding, and flip chip or controlled collapse chip connection (C4) have been developed and widely used; and

3) Package and device sealing: chips and carriers are covered or sealed by resin, ceramic or other packaging material to protect the devices on the chips and the connections between the chips and the carriers.

First Embodiment

In Fig. 3A and Fig. 3B, cross sectional view of a multi-chip chip-scale package is shown. In the invention, a lead frame is in use as a carrier. Typically, the lead frame comprises a die pad 50 and several leads 56. The leads 56 are further categorized into a part of inner leads 52 and the other part of outer leads 54. Multiple chips 58, 60, 62, 64 and 66 are packed into a package with a volume about the same of a total volume of all these chips 58 to 66. The chips 58 to 66 may include DRAM, read only memory (ROM), LOGIC or ANALOG circuits, or other devices. Each of the chips 58 to 66 has a surface 58a to 66a, respectively, which comprise several pads 68. The invention adapts the flip chip technique. A bump 70 is formed on each pad 68. The chips 58 to 66 are disposed face-to-face and electrically connected with each other via the bumps 70. Since the flip-chip technique is employed, the pads 68 can be designed with an area array layout distributed on the chips 58 to 66. The design can thus be applied in a semiconductor with a high integration and many I/O nodes.

Regarding to the electrical connection between the chips 58 to 66 and the lead frame, a conventional wire bonding can be used. Using thread-like conductive

material 72, for example, gold, aluminum threads or other metal threads or conductive wires, a part of the pads 68 are connected to the inner leads 52. Or alternatively, using flip-chip technique, the bumps 70 is electrically connected to the inner leads 52 (as shown in Fig. 3B). A filling material 74, for example, insulation material such as epoxy is filled between the chips 58 to 66. An anisotropic conductive paste (ACP) may also be used to improve the performance of electrical connection between bumps 70. For the packaging and molding part, insulation material 76 such as epoxy is used to seal the die pad 50, the chips 58 to 66, and the inner leads 52.

Referring to Fig. 3C and 3D, a face-to-face multi-chip package with a heat dissipation apparatus is shown. Considering the heat dissipation of the package, the rear surfaces 58b, 60b of the chips 58, 60 are bared (as shown in Fig. 3C). In this way, the thickness of the package is reduced, and a better path for heat dissipation is provided. For further enhancing the performance of heat dissipation, a heat dissipation apparatus 78a such as a heat spreader or a heat sink can be further disposed above the rear surfaces 58b to 62b of the chips 58 to 62. Or another heat dissipation apparatus 78b, for example, a heat spreader or a heat sink, can be disposed above the rear surface of the die pad 78b and exposed outside of the insulation material 76.

The subsequent step for forming the leads 56, and the surface mount technique (SMT) used at the junction between the leads 56 and the circuit board are conventional. The detailed description is thus omitted here.

It is appreciated that people skilled in the art may also apply a lead frame without a die pad, for example, a lead on chip (LOC) or chip on lead (COL) structures, to replace the typical lead frame.

Second Embodiment

In Fig. 4A, a cross sectional view of a multi-chip chip-scale package is shown. In the invention, a film carrier is in use. Typically, the lead frame comprises a flexible film 80 and several leads 56. The leads 86 are further categorized into a part of inner leads 82 and the other part of outer leads 84. Each of the chips 58, 60, 62, 64 and 66 having a surface 58a, 60a, 62a, 64a, and 66a, respectively, which comprise several pads 68. The invention adapts the flip chip technique. A bump 70 is formed on each pad 68. The chips 58 to 66 are disposed face-to-face and electrically connected with each other via the bumps 70. Since the flip-chip technique is employed, the pads 68 can be designed with an area array layout distributed on the chips 58 to 66. The design can thus be applied in a semiconductor with a high integration and many I/O nodes.

Regarding to the electrical connection between the chips 58 to 66 and the leads 86, the flip-chip technique can be used. The bumps 70 are electrically connected to the leads 86. A filling material 74, for example, insulation material such as epoxy is filled between the chips 58 to 66. An anisotropic conductive paste (ACP) may also be used to improve the performance of electrical connection between bumps 70. For the packaging and molding part, an insulation material 76 such as epoxy is used to seal the chips 58 to 66, and the inner leads 82.

Referring to Fig. 4C and 4D, a face-to-face multi-chip package with a heat dissipation apparatus is shown. Considering the heat dissipation of the package, some or all of the rear surfaces 58b, 60b, 62b, 64b, and 66b of the chips 58 to 66 are bared (as shown in Fig. 4B). In this way, the thickness of the package is reduced, and a better path for heat dissipation is provided. For further enhancing the performance of heat

dissipation, a heat dissipation apparatus 88a such as a heat spreader or a heat sink can be further disposed above the rear surfaces 58b to 62b of the chips 58 to 62. Or another heat dissipation apparatus 88b, for example, a heat spreader or a heat sink, can be disposed above the rear surfaces 64b and 66b of the chips 64 and 66 and exposed outside of the insulation material 76.

In the subsequent step for forming the leads 86, and the surface mount technique (SMT) used at the junction between the leads 86 and the circuit board are conventional. The detailed description is thus omitted here.

Third Embodiment

In Fig. 5A, another face-to-face multi-chip package is shown. A printed circuit board (PCB) or a glass is used as a carrier. Typically, a PCB or glass carrier comprises a substrate 90, for example, FR-4, FR-5, BT or glass substrate. The substrate 90 has several terminals 92. While a PCB is in used, the chip-on-board (COB) technique or a substrate comprising a BGA is employed for packaging. The substrate 90 is formed of lamination of layers of insulation material or printed circuits (copper foils). The chips 58, 60, 62, 64, 66 each has a surface 58a, 60a, 62a, 64a, 66a, respectively. Several pads 68 are formed on each of the surfaces 58a to 66a. The connections between the chips 58 to 66 adapt the flip chip technique. Bumps 70 are formed on each of the pads 68. The chips 58 to 66 are face-to-face disposed and electrically connected with each other via bumps 70. Since the flip-chip technique is adapted, the pads 68 can be distributed on the chips 58 to 66 in an area array. It can therefore be applied in a semiconductor with a high integration and many I/O nodes.

Referring to Fig. 5C and 5D, a face-to-face multi-chip package with a heat

dissipation apparatus is shown. Considering the heat dissipation of the package, some or all of the rear surfaces 58b, 60b, 62b, 64b, and 66b of the chips 58 to 66 are bared. As shown in Fig. 5C, the bared surfaces comprise 58b and 60b. In this way, the thickness of the package is reduced, and a better path for heat dissipation is provided. For further enhancing the performance of heat dissipation, a heat dissipation apparatus 98 such as a heat spreader or a heat sink can be further disposed above the rear surfaces 58b and 66b of the chips 58 and 66. The heat dissipation apparatus 98 is exposed outside of the insulation material 76.

In summary, the advantages of the invention includes at least:

1) The thickness and surface area are reduced by the application of face-to-face multi-chip package. By the employment of flip-chip technique, the pads can be designed as an area array, so that the integration is greatly enhanced.

2) Bumps are formed to achieve the electrical connections between chips, the signal transmission is thus shortened. The performance of the package is thus improved. With the area array layout of the pads, the package can be applied to a semiconductor with a further increased integration and many I/O nodes.

3) The invention may also adapt a bared-chip package, so that the performance of heat dissipation is improved. Furthermore, a heat dissipation can be further installed to further enhance the heat dissipation.

4) The package can be applied to chips including DRAM, ROM, SRAM, Flash Memory, LOGIC or ANALOG circuits. Thus, the field of application is so wide to include apparatus with various functions or frequency, such as communication equipment or computer system, or even a single system chip.

Other embodiments of the invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples to be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.



WHAT IS CLAIMED IS:

1. A face-to-face multi-chip chip package, comprising:

a lead frame, comprising at least a die pad and a plurality of leads, the leads further comprising a plurality of inner leads and a plurality of outer leads;

a plurality of chips, each having a surface comprising a plurality of pads, the chips being disposed with the surfaces comprising the pads face to face;

a plurality of bumps, disposed on the pads to electrically connect the chips;

a plurality of conductive materials, connecting the pads and the inner leads; and

an insulation material, sealing the die pad, the chips and the inner leads.

2. The package according to claim 1, wherein an epoxy resin is filled between the chips.

3. The package according to claim 1, wherein an anisotropic conductive paste is filled between the chips.

4. The package according to claim 1, wherein the conductive material comprises metal threads.

5. The package according to claim 1, wherein conductive material comprises bumps.

6. The package according to claim 1, wherein the insulation material

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comprises epoxy.

7. The package according to claim 5, wherein the pads are distributed on the chips as an area array.

8. The package according to claim 1, wherein the chips have another bared surfaces.

9. The package according to claim 8, wherein a heat dissipation apparatus is further installed on the bared surfaces of the chips.

10. The package according to claim 1, wherein a heat dissipation apparatus is further installed on the die pad and exposed outside of the insulation material.

11. A face-to-face multi-chip package, comprising:

a substrate, the substrate having a surface comprising a plurality of terminals;

a plurality of chips, disposed on the substrate, each of the chips comprising a surface on which a plurality of pads are formed, the chips being disposed face to face with the surface comprising the pads;

a plurality of bumps, disposed on the pads to electrically connect the chips;

a plurality of conductive wires, connecting the pads and the substrate; and

an insulation material, sealing the substrate and the chips.

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12. The package according to claim 11, wherein substrate comprises a ball grid array package substrate.

13. The package according to claim 11, wherein the substrate comprises a printed circuit board.

14. The package according to claim 11, wherein the substrate comprises a glass.

15. The package according to claim 11, wherein an epoxy resin is further filled between the chips.

16. The package according to claim 11, wherein an anisotropic conductive paste is further filled between the chips.

17. The package according to claim 11, wherein the insulation material comprises epoxy resin.

18. The package according to claim 11, wherein the insulation material seals a part of the substrate and the chips, while each of the chips has a bared surface.

19. The package according to claim 11, wherein the pads are distributed on the chips as an area array.



20. The package according to claim 11, wherein a heat dissipation apparatus is further installed on the bared surfaces of the chips and exposed outside of the insulation material.

21. A face-to-face multi-chip package, comprising:

a carrier, comprising a plurality of inner leads and a plurality of outer leads;

a plurality of chips, each having a surface on which a plurality of pads, the chips being disposed face to face with the surface comprising the pads;

a plurality of first bumps, disposed on the pads to electrically connect the chips;

a plurality of second bumps, to connect a part of the pads and the inner leads; and

an insulation material, sealing the chips and the inner leads.

22. The package according to claim 21, wherein the carrier comprises a lead frame.

23. The package according to claim 21, wherein the carrier comprises a film carrier.

24. The package according to claim 21, wherein an epoxy resin is further filled between the chips.

25. The package according to claim 21, wherein an anisotropic conductive

paste is filled between the chips.

26. The package according to claim 21, wherein the insulation material comprises epoxy resin.

27. The package according to claim 21, wherein the pads are distributed on the pads as an area array.

28. The package according to claim 21, wherein the insulation material exposes another surface of each of the chips.

29. The package according to claim 21, wherein a heat dissipation apparatus is further installed on another side of the chips and exposed outside of the insulation material.