

CLAIMS

1. An apparatus, comprising:
a memory cell configured to store a logic state;
a first memory access line coupled to the memory cell; and
a second memory access line coupled to the memory cell,
wherein the first and second memory access lines are configured to provide a first voltage having a first polarity across the memory cell to write a first logic state to the memory cell and provide a second voltage having a second polarity across the memory cell to write a second logic state to the memory cell,
wherein, during a read operation on the memory cell, the memory cell exhibits a first threshold voltage representative of the first logic state responsive to the first voltage having the first polarity provided to write to the memory cell,
or the memory cell exhibits a second threshold voltage representative of the second logic state responsive to the second voltage having the second polarity provided to write to the memory cell.
2. The apparatus of claim 1, wherein the memory cell comprises a chalcogenide material.
3. The apparatus of claim 2, wherein the chalcogenide material is not a phase change material.
4. The apparatus of claim 1, wherein the memory cell comprises at least one of silicon (Si), selenium (Se), arsenic (As), and germanium (Ge).
5. An apparatus, comprising:
a memory cell configured to store a logic state, wherein the memory cell is a two-terminal threshold switching device;
a first memory access line coupled to the memory cell; and
a second memory access line coupled to the memory cell,

wherein the first and second memory access lines are configured to provide a first voltage having a first polarity across the memory cell to write a first logic state to the memory cell and provide a second voltage having a second polarity across the memory cell to write a second logic state to the memory cell.

6. The apparatus of claim 1, wherein the memory cell comprises a selector device coupled to the first memory access line and a memory element coupled to the selector device and the second memory access line.

7. The apparatus of claim 1, wherein the first memory access line is configured to provide a negative voltage and the second memory access line is configured to provide a positive voltage to provide the first voltage having the first polarity.

8. The apparatus of claim 1, wherein the first memory access line is configured to provide a first non-negative voltage and the second memory access line is configured to provide a second non-negative voltage to provide the first voltage having the first polarity, wherein the second non-negative voltage is greater than the first non-negative voltage.

9. An apparatus, comprising:

a memory cell configured to exhibit a first threshold voltage when in a first logic state and a second threshold voltage when in a second logic state responsive to a read operation, wherein the memory cell is further configured to act as a memory element and a selector device;

a first memory access line coupled to the memory cell; and

a second memory access line coupled to the memory cell,

wherein the first and second memory access lines are configured to provide a read pulse during the read operation, the read pulse having a first polarity,

wherein the first and second memory access lines are further configured to provide a write pulse having the first polarity or a second polarity during a write operation.

10. The apparatus of claim 9, wherein the first memory access line is configured to provide a negative voltage and the second memory access line is configured to provide a positive voltage to provide the write pulse having the first polarity.

11. The apparatus of claim 9, wherein the first memory access line is configured to provide a first non-negative voltage and the second memory access line is configured to provide a second non-negative voltage to provide the write pulse having the first polarity, wherein the second non-negative voltage is greater than the first non-negative voltage.

12. The apparatus of claim 9, wherein the memory cell exhibits the first threshold voltage responsive to the read operation when the write pulse having the first polarity was provided during the write operation and the memory cell exhibits the second threshold voltage responsive to the read operation when the write pulse having the second polarity was provided during the write operation.

13. The apparatus of claim 9, further comprising a memory array including a plurality of memory cells and a plurality of memory access lines coupled to at least some of the plurality of memory cells,

wherein the memory cell is one of the plurality of memory cells and the first and second memory access lines are each one of the plurality of memory access lines.

14. The apparatus of claim 13, wherein the memory array is a two-dimensional array.

15. The apparatus of claim 13, wherein the memory array is a three-dimensional array.

16. The apparatus of claim 9, further comprising:
a first electrode coupled between the memory cell and the first memory access line; and
a second electrode coupled between the memory cell and the second memory access line.
17. The apparatus of claim 9, further comprising a sense amplifier coupled to the first memory access line or the second memory access line, the sense amplifier configured to sense a current through the memory cell responsive to the read operation.
18. The apparatus of claim 9, wherein the memory cell comprises a chalcogenide.
19. A method, comprising:
applying a first read pulse having a first polarity to a memory cell, wherein the memory cell was programmed to a logic state with a write pulse having the first polarity or a second polarity;
sensing a first threshold voltage of the memory cell responsive to the first read pulse;
applying a second read pulse having the first polarity to the memory cell;
sensing a second threshold voltage of the memory cell responsive to the second read pulse;
calculating a difference between the first threshold voltage and the second threshold voltage; and
determining the logic state of the memory cell, wherein the logic state is determined to be a first state when the difference is below a threshold value and the logic state is determined to be a second state when the difference is above the threshold value.
20. The method of claim 19, wherein the first and second read pulses are ramped voltage pulses.

21. The method of claim 20, wherein a voltage of the ramped voltage pulses is increased linearly.

22. The method of claim 20, wherein a voltage of the ramped voltage pulses is increased non-linearly.

23. The method of claim 19, further comprising reprogramming the memory cell to the logic state after the second read pulse.