CLAIMS

1. A memory, comprising: a first global word line; a first set of bit lines; a first local word line; a first set of memory cells coupled to the first local word line and coupled to the first set of bit lines, respectively; a first local word line driver configured to generate a first asserted signal on the local word line in response to receiving a second asserted signal from the first global word line and a third asserted signal; a first set of bit line drivers configured to apply programming voltages on the first set of bit lines based on a first set of bit line programming signals, respectively; and a multiple-input OR-gate configured to generate the third asserted signal in response to at least one of the first set of bit line programming signals being asserted.

2. The memory of claim 1, wherein the third asserted signal indicates that at least one of the programming voltages is applied to at least one of the first set of bit lines for programming at least one of the first set of memory cells, respectively.

3. The memory of claim 1, wherein the first asserted signal is configured to effectuate the programming of the at least one of the first set of memory cells.

4. The memory of claim 1, further comprising a sense amplifier coupled to the first set of bit lines, wherein the first asserted signal is configured to effectuate a reading of data from the first set of memory cells by the sense amplifier.

5. The memory of claim 4, wherein the first set of bit line drivers are configured to be tri-stated during the reading of the data from the first set of memory cells by the sense amplifier.

6. The memory of claim 1, wherein at least one of the first set of memory cells is configured as an EFUSE memory cell.

7. The memory of claim 1, wherein at least one of the first set of memory cells comprises a fuse element coupled in series with a transistor between a corresponding one of the first set of bit lines and a voltage rail.

8. The memory of claim 1, wherein at least one of the first set of memory cells is configured as an antifuse memory cell.

9. The memory of claim 1, wherein at least one of the first set of memory cells each includes at least one core device.

10. The memory of claim 1, further comprising: a second local word line; a second set of bit lines; a second set of memory cells coupled to the second local word line and coupled to the second set of bit lines, respectively; and a second local word line driver configured to generate a fourth asserted signal on the second local word line in response to receiving the second asserted signal from the first global word line and a fifth asserted signal.

11. The memory of claim 1, further comprising: a second global word line; a second local word line; a second set of memory cells coupled to the second local word line and coupled to the first set of bit lines, respectively; and a second local word line driver configured to generate a fourth asserted signal on the second local word line in response to receiving a fifth asserted signal from the second global word line and the third asserted signal.

12. The memory of claim 1, further comprising a word line decoder including a global word line driver configured to generate the second asserted signal.

13. The memory of claim 12, wherein the global word line driver is configured to: generate the second asserted signal at a first voltage for effectuating a programming of at least one of the first set of memory cells; or generate the second asserted signal at a second voltage for effectuating a reading of data from at least one of the first set of memory cells.

14. A method, comprising: generating a first asserted signal on a global word line; generating a second asserted signal; generating a third asserted signal on a local word line for accessing at least one of a set of memory cells in response to receiving the first asserted signal from the global word line and the second asserted signal; generating at least one programming voltage on a set of bit lines based on a set of bit line programming signals, respectively; and performing a logical OR operation of the bit line programming signals to generate the second asserted signal.

15. The method of claim 14, wherein the third asserted signal indicates that the least one of the programming voltage is applied to at least one of the set of bit lines coupled to the set of memory cells, respectively.

16. The method of claim 14, wherein the third asserted signal is configured to effectuate the programming of the at least one of the set of memory cells.

17. The method of claim 14, further comprising generating a fourth asserted signal configured to effectuate a reading of data from the at least one of the set of memory cells, wherein the fourth asserted signal is generated in response to a fifth asserted signal from the global word line and a sixth asserted signal.

18. The method of claim 14, wherein at least one of the set of memory cells is configured as an EFUSE memory cell.

19. The method of claim 14, wherein at least one of the set of memory cells is configured as an antifuse memory cell.

20. The method of claim 14, wherein at least one of the set of memory cells each includes at least one core device.

21. An apparatus, comprising: means for generating a first asserted signal on a global word line; means for generating a second asserted signal; means for generating a third asserted signal on a local word line for accessing at least one of a set of memory cells in response to receiving the first asserted signal from the global word line and the second asserted signal; means for generating at least one programming voltage on a set of bit lines based on a set of bit line programming signals, respectively; and means for performing a logical OR operation of the bit line programming signals to generate the second asserted signal.

22. The apparatus of claim 21, wherein the third asserted signal indicates that a programming voltage is applied to at least one of the set of bit lines for programming the at least one of the set of memory cells.

23. The apparatus of claim 21, wherein the third asserted signal is configured to effectuate the programming of at least one of the set of memory cells.

24. The apparatus of claim 21, further comprising means for generating a fourth asserted signal configured to effectuate a reading of data from at least one of the set of memory cells, wherein

the fourth asserted signal is generated in response to the fifth asserted signal from the global word line and a sixth asserted signal.

25. The apparatus of claim 21, wherein at least one of the set of memory cells is configured as an EFUSE memory cell.

26. The method of claim 21, wherein at least one of the set of memory cells is configured as an antifuse memory cell.

27. The apparatus of claim 21, wherein at least one of the set of memory cells includes at least one core device.