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(54) DIGITAL ELECTRONIC TIMEPIECE

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to digital electronic timepieces.

In conventional electronic timepieces, if seconds, minutes, hours, date and month are displayed by a single display panel, it is necessary to provide the display panel with a display portion consisting of two alphanumeric display units for the seconds, a display portion consisting of four alphanumeric display units for the minutes and hours, and a display portion consisting of four alphanumeric display units for the date and month. Thus the display panel must have a total of ten alphanumeric display units. If the alphanumeric display units are to be read easily, then the display panel has to be relatively large. Therefore, it is very difficult to make a ladies' wristwatch of this type which is also of small size.

To overcome this problem it has been suggested that four alphanumeric display units are employed so that date and months, hours and minutes, and seconds may be selectively displayed. This enables the size of the display panel to be reduced, but it is difficult to determine the information being displayed at any given time, unless the electronic timepiece is provided with additional circuitry for producing an additional display indicative of the information being displayed at any given time. The mounting of the additional display has a disadvantage that it is impossible to see the display from the stand point perspective. A small sized wristwatch has also been suggested having two alphanumeric display units instead of four by means of which seconds, minutes, hours, date and month are selectively displayed.

According to the present invention there is provided a digital electronic timepiece comprising: a time signal pulse generating circuit;

a time counting circuit for generating time signals corresponding to seconds, minutes, hours and date; a liquid crystal display means having retardation effect for displaying a digital time unit signal in different colours according to the drive voltage applied; a first switching circuit for selectively supplying different time unit signals from said time counting circuit to said display means for visual display thereby; a voltage level circuit for producing a plurality of different drive voltages for driving said liquid crystal display means; and a second switching circuit means coordinated with said first switching circuit means to supply from said voltage level circuit to said display means a selected drive voltage corresponding to a selected time unit signal to be displayed so that different time unit signals are distinguished from one another by being displayed in different colours.

In a preferred embodiment said display means consists of means for displaying two digits.

The digital electronic timepiece may include manually operable switch means for jointly controlling said first switching circuit means and said second switching circuit means.

Preferably the digital electronic timepiece includes a driving circuit for driving said display means, said driving circuit having inputs connected respectively to said first switching circuit means and said second switching circuit means and outputs connected to said display means.

In the preferred embodiment said voltage level circuit comprises means for providing four different drive voltages. Preferably said display means comprises segment electrodes and a figure electrode said driving circuit comprising means controlled by voltage pulse supplied by said time signal pulse generating circuit for supplying a selected drive voltage alternately to selected ones of said segment electrodes and said figure electrode to display a selected time signal in a selected colour.

The invention is illustrated, merely by way of example, in the accompanying drawings in which:—

Figure 1 is a block diagram of one em-

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bodiment of a digital electronic timepiece according to the present invention;

Figure 2 illustrates graphically the retardation effect of a liquid crystal material;

Figure 3 is a circuit diagram of a voltage level circuit for the digital electronic timepiece of Figure 1;

Figure 4 is a circuit diagram of a first switching circuit of the digital electronic timepiece of Figure 1;

Figure 5 is a circuit diagram of a second switching circuit of the digital electronic timepiece of Figure 1; and

Figure 6 is a circuit diagram of a drive circuit of the digital electronic timepiece of Figure 1.

Referring first to figure 1, there is shown, in block diagram form, a digital electronic timepiece according to the present invention. A time-keeping circuit 1 includes an oscillator circuit (not shown) controlled by a quartz crystal vibrator element and which produces a relatively high frequency signal, a dividing circuit (not shown) for frequency dividing the relatively high frequency signal from the oscillator circuit and producing a relatively low frequency standard time signal having a frequency of, for example, 1Hz, a time counter circuit (not shown) for producing timing signals corresponding to time units of seconds, minutes, hours, day of the week, days of the month and months by counting the pulses of the standard time signal, and a decoder circuit (not shown) for converting the timing signals from the time counter circuit into coded time signals. Therefore, four kinds of time unit signals are produced at the output of the time keeping circuit 1. The time keeping circuit 1 is driven by the output voltage from a voltage boosting circuit 3 and by the battery voltage of a battery 2. A voltage level circuit 4 generates four different voltage levels.

One embodiment of the voltage level circuit 4 is illustrated in Figure 3. The voltage produced by the voltage boosting circuit 3 appears at terminal a_1 , a voltage which is less than the voltage produced by the voltage boosting circuit and determined by a resistor R_1 and a zener diode ZD_1 appears at terminal a_2 , a voltage which is less than the voltage appearing at the terminal a_2 and determined by a resistor R_2 and a zener diode ZD_2 appears at terminal a_3 and a voltage which is less than the voltage appearing at terminal a_3 and determined by a resistor R_3 and a zener diode ZD_3 appears at a terminal a_4 . The voltages appearing at the terminals a_2 , a_3 , a_4 are determined by the zener voltages of the zener diodes ZD_1 , ZD_2 , ZD_3 , the resistance values of the resistors R_1 , R_2 , R_3 determining the electric current flowing to the zener diodes.

Referring back to figure 1, the time units signals produced by the time keeping circuit 1 are applied to a switching circuit 5 and the four voltage levels produced by the voltage level circuit 4 are applied to a switching circuit 6. The switching circuits 5, 6 are controlled by a rotary mechanical switch 7, for example, operated by a stem member (not shown) of the digital electronic timepiece. The switching circuit 5 selects one of the time unit signals from the time keeping circuit 1 and applies it to a driving circuit 8. The switching circuit 7 selects one of the four voltage levels from the voltage level circuit 4 and also applies it to the driving circuit 8. When the switching circuit 5 selects the time signal corresponding to months, the switching circuit 6 selects the voltage appearing at the terminal a_1 of the voltage level circuit 4. When the time unit signal corresponding to days of the month is selected, the voltage appearing at the terminal a_2 is selected by the switching circuit 6. When the time unit signal corresponding to hours is selected, the voltage appearing at the terminal a_3 is selected by the switching circuit. When the time signal corresponding to minutes is selected, the voltage appearing at the terminal a_4 is selected by the switching circuit 6.

The driving circuit 8 drives a liquid crystal display device 9 with the voltage selected by the switching circuit 6, the time unit signal selected by the switching circuit 5 being displayed by the display of the liquid crystal display device 9. The liquid crystal display device 9 is composed of two alphanumeric display units each having seven segments and a common electrode. The liquid crystal material employed in the liquid crystal display device 9 exhibits the retardation effect, so that its colour is dependent upon the driving voltage.

The retardation effect of a liquid crystal material will be explained in relation to Figure 2. In Figure 2, the abscissa indicates the drive voltage applied to the liquid crystal material and the ordinate indicates the transmitted light intensity transmitted through the liquid crystal material. The curved lines, G, B, R indicate the change of intensity of transmitted light for green, blue and red light respectively. At a voltage V_1 the transmitted intensity of red light is a maximum so that the liquid crystal material will appear red in colour. At a voltage V_2 the transmitted intensity of blue light is a maximum so that the liquid crystal material will appear blue in colour. At a voltage V_3 the transmitted intensity of green light is the maximum so that the liquid crystal material will appear green in colour. If a voltage between V_1 and V_2 is applied to the liquid crystal material, the liquid crystal material will appear to have a colour between red and blue, namely red-blue, purple and blue-purple. It will be appreciated that the display produced by the liquid crystal display device 9 is thus easily changed by changing the driving voltage.

When one of the time unit signals is selected

by the switching circuit 5, the drive voltage for the liquid crystal display device 9 is selected by the switching circuit 6 so that when the time unit signal being displayed by the liquid crystal display device 9 is changed, the colour display is simultaneously changed. By this means it is possible for a user to appreciate immediately the information being displayed by the liquid crystal display device 9.

Figure 4 illustrates in detail the switching circuit 5. The switching circuit 5 has gate circuits 10A, 10B, 11A, 11B, 12A, 12B, 13A, 13B each consisting of seven AND circuits 14a to 14g, only the AND circuits of gate circuit 10A, 10B being shown. Segment signals of which the time unit signal corresponding to minutes produced by the time keeping circuit 1 is composed, are applied to a respective one input terminal of each of the AND circuits 14a to 14g of the gate circuits 10A, 10B, the other input terminals being commonly connected to a stationary contact 18 of the mechanical switch 7. Segment signals of the time unit signal corresponding to hours produced by the time keeping circuit 1 are applied to one input terminal of the AND circuits 14a to 14g of the gate circuits 11A, 11B, the other input terminals being commonly connected to a stationary contact 19 of the mechanical switch 7. Segment signals of the time unit signal corresponding to days of the month produced by the time keeping circuit 1 are applied to one input terminal of the AND circuits 14a to 14g of the gate circuits 12A, 12B, the other input terminals being commonly connected to a stationary contact 20 of the mechanical switch 7. Segment signals of the time signal corresponding to months produced by the time keeping circuit 1 are applied to one input terminal of the AND circuits 14a to 14g of the gate circuits 13A, 13B, 13C the other input terminals being commonly connected to a stationary contact 21 of the mechanical switch 7. The mechanical switch 7 has a movable contact 22 which may be selectively brought into electrical contact with stationary contacts 18, 19, 20, 21. The movable contact 22 is connected to a terminal 23 which is at a voltage level corresponding to logic "1". The outputs of the gate circuits 10A, 11A, 12A, 13A are applied to a gate circuit 15A. The outputs of the gate circuits 10B, 11B, 12B, 13B are applied to a gate circuit 15B. The gate circuits 15A, 15B, are each composed of four-input OR circuits 16a to 16g. The output of the AND circuits of 14a of the gate circuits 10A, 11A, 12A, 13A are applied to the OR circuit 16a of the gate circuit 15A, the output of the AND 14g of the gate circuit, 10B, 11B, 12B, 13B are applied to OR circuit 16g of the gate circuit 15B. The outputs of the OR circuits 16a to 16g of the gate circuit 15A are connected to terminals 17Aa to 17Ag which form output terminals of the switching circuit 5.

The outputs of the OR circuits 16a to 16g of the gate circuit 15B are connected to terminals 17Ba to 17Bg which also form output terminals of the switching circuit 5.

When the movable contact 22 of the mechanical switch 7 is in electrical contact with the stationary contact 21, the segment signals of the time unit signal corresponding to months generated from the time keeping circuit 1 passes through the gate circuits 13A, 13C, the gate circuits 15A, 15B, and appear at the terminals 17Aa to 17Ag and 17Ba to 17Bg. In the same manner when the movable contact 22 is in electrical contact with the stationary contact 20, the segment signals of the time unit signal corresponding to minutes passes through the gate circuits 12A, 12B, 15A, 15B and appear at the terminals 17Aa to 17Ag, and 17Ba to 17Bg. According to the position of mechanical switch 7, the segment signals of the time unit signals corresponding to minutes, hours, day of the month, and months, appear at the output terminals 17Aa to 17Ag and 17Ba to 17Bg of the switching circuit 5.

Figure 5 illustrates, in detail, the switching circuit 6. The switching circuit 6 has four transmission gates 24, 25, 26, 27 and four inverters 28, 29, 30, 31. Input terminals of the transmission gates 24, 25, 26, 27 are respectively connected to the terminals a_1, a_2, a_3, a_4 of the voltage level circuit 4 and the output terminals of the transmission gates 24, 25, 26, 27 are commonly connected to a terminal 32 which forms the output terminals of switching circuit 6. One control terminal of each transmission gate 24, 25, 26, 27 is connected to one of the stationary terminals, 18, 19, 20, 21 of the mechanical switch 7. The inverters 28, 29, 30, 31 are respectively connected between the control terminals of the transmission gates. The voltage appearing at the terminals a_1 , namely the highest voltage, of the voltage level circuit 4 is applied to the terminal 23 permanently in contact with the movable contact 22 of the mechanical switch 7.

When the movable contact 22 of the mechanical switch 7 is in electrical contact with the stationary contact 20 the transmission gate 25 becomes conductive so that the voltage at the terminal a_2 of the voltage level circuit 4 appears at the terminal 32. When the transmission gates 24, 25, 26, 27 are respectively conductive upon operation of the mechanical switch 7, the four voltage levels produced by the voltage level circuit 4 selectively appear at the terminal 32.

Figure 6 shows in detail, the drive circuit 8 of Figure 1. The drive circuit of Figure 6 is for one of the alphanumeric display units of the liquid crystal display device 9, however, a drive circuit for the other alphanumeric display unit is of the same construction.

To one input of exclusive OR circuits 33a

to 33g are applied the segment signals appearing at the terminals 17Aa to 17Ag of the switching circuit 5. A dividing signal having a frequency of, for example, 32 Hz and obtained from the time keeping circuit 1 is applied to a terminal 34 and to the other input of the exclusive OR circuits 33a to 33g. The outputs of the exclusive OR circuits 33a to 33g are increased to the voltage level at terminal a₁ of the voltage level circuit 4, namely the output voltage of the voltage boosting circuit 3 by level shifters 35a to 35g and are respectively applied directly to one control terminal of a respective pair of transmission gates 36a to 36g and 37a to 37g and are applied to the other control terminal *viz* inverters 38a to 38g. The input terminal of the transmission gates 36a to 36g are connected in common to the terminal 32 of the switching circuit 6, and the output terminals are respectively connected to segment electrodes a to g in the alphanumeric display unit of the liquid crystal display device 9. The dividing signal applied to the terminal 34 is increased to the amplitude of the output voltage of the voltage boosting circuit 3 by a level shifter 39 and is applied directly to one control terminal of a pair of transmission gates 40, 41 and is inverted by an inverter 42 and is applied to the other control terminal. The input terminal of the transmission gate 40 is connected to the terminal 32, and the input terminal of the transmission gate 41 is connected to earth. The output terminals of the pair of transmission gates 40, 41 are connected in common to a figure electrode X of the alphanumeric display unit of the liquid crystal display device 9.

When a segment signal of level H (high) appears at the terminal 17Aa, and the dividing signal applied to the terminal 34 is level H, the outputs of the exclusive OR circuit 33a and the level shifter 35a are level L (low) whereby the transmission gate 36a becomes conductive and the voltage level at the terminal 32 is applied to the segment electrode a. When the signal applied to the terminal 34 is at level H, the transmission gate 41 is conductive whereby the voltage on the electrode X becomes logical "0". On the other hand, when the signal applied to the terminal 34 is level L the transmission gate 37a becomes conductive whereby the voltage of the segment electrode a becomes logical "0" and furthermore the transmission gate 40 becomes conductive so that the voltage level of the terminal 32 is applied to the electrode X. Therefore, during the time when the segment signal is level H the voltage at the terminal 32 is alternately in time applied to the segment a and the electrode X in synchronism with the frequency of the signal applied to the terminal 34 whereby the liquid crystal material between the segment electrode a and the electrode X is continually driven by alternating current.

When a segment signal does not appear at the terminal 17Aa it is at level L, the transmission gate 37a therefore becomes conductive when the signal applied to the terminal 34 is at level H so that the segment electrode a is logical "0" as also is the electrode X. The voltage at the terminal 32 is applied to the segment electrode a and to the electrode X when the signal applied to the terminal 34 is level L because the transmission gate 36a is conductive. Therefore, no electric field exists between the segment electrode a and the electrode X so that the liquid crystal material therebetween is not driven.

The other segment electrodes b to g are operated in a similar manner. Further, the voltage of the terminal 32 namely, one of the voltages appearing at the terminals a₁, a₂, a₃, a₄ of the voltage level circuit 4 is selected by the switching circuit 6.

The liquid crystal display device 9, in this embodiment, may selectively have any one of four colours. Therefore, monuths, days of the month, hours and minutes are selectively displayed by the liquid crystal display device 9, and simultaneously with change of information displayed, the colour of the display changes. Thus the user can easily distinguish the information being displayed at any given instant.

It is possible to make the liquid crystal display device 9 display seconds by employing a further voltage level by the voltage level circuit 4. Further, it is possible to display months and days of the month simultaneously in the same colour or different colours by employing a liquid crystal display device having four alphanumeric display units, and similarly to display hours and minutes in the same or different colours, again by employing four alphanumeric display units. It will be appreciated that it is, therefore, easy to distinguish between a display of month and days of the month, and a display of hours and minutes.

In the place of the mechanical switch 7, it is possible to display cyclically the time signals by employing a signal obtained from a given dividing stage of the dividing circuit which forms part of the time keeping circuit 1.

WHAT WE CLAIM IS:—

1. A digital electronic timepiece comprising: a time signal pulse generating circuit; a time counting circuit for generating time signals corresponding to seconds, minutes, hours and date; a liquid crystal display means having retardation effect for displaying a digital time unit signal in different colours according to the drive voltage applied; a first switching circuit for selectively supplying different time unit signals from said time counting circuit to said display means for visual display thereby; a voltage level circuit for producing a plurality of different drive voltages

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to 33g are applied the segment signals appearing at the terminals 17Aa to 17Ag of the switching circuit 5. A dividing signal having a frequency of, for example, 32 Hz and obtained from the time keeping circuit 1 is applied to a terminal 34 and to the other input of the exclusive OR circuits 33a to 33g. The outputs of the exclusive OR circuits 33a to 33g are increased to the voltage level at terminal a₁ of the voltage level circuit 4, namely the output voltage of the voltage boosting circuit 3 by level shifters 35a to 35g and are respectively applied directly to one control terminal of a respective pair of transmission gates 36a to 36g and 37a to 37g and are applied to the other control terminal *viz* inverters 38a to 38g. The input terminal of the transmission gates 36a to 36g are connected in common to the terminal 32 of the switching circuit 6, and the output terminals are respectively connected to segment electrodes a to g in the alphanumeric display unit of the liquid crystal display device 9. The dividing signal applied to the terminal 34 is increased to the amplitude of the output voltage of the voltage boosting circuit 3 by a level shifter 39 and is applied directly to one control terminal of a pair of transmission gates 40, 41 and is inverted by an inverter 42 and is applied to the other control terminal. The input terminal of the transmission gate 40 is connected to the terminal 32, and the input terminal of the transmission gate 41 is connected to earth. The output terminals of the pair of transmission gates 40, 41 are connected in common to a figure electrode X of the alphanumeric display unit of the liquid crystal display device 9.

When a segment signal of level H (high) appears at the terminal 17Aa, and the dividing signal applied to the terminal 34 is level H, the outputs of the exclusive OR circuit 33a and the level shifter 35a are level L (low) whereby the transmission gate 36a becomes conductive and the voltage level at the terminal 32 is applied to the segment electrode a. When the signal applied to the terminal 34 is at level H, the transmission gate 41 is conductive whereby the voltage on the electrode X becomes logical "0". On the other hand, when the signal applied to the terminal 34 is level L the transmission gate 37a becomes conductive whereby the voltage of the segment electrode a becomes logical "0" and furthermore the transmission gate 40 becomes conductive so that the voltage level of the terminal 32 is applied to the electrode X. Therefore, during the time when the segment signal is level H the voltage at the terminal 32 is alternately in time applied to the segment a and the electrode X in synchronism with the frequency of the signal applied to the terminal 34 whereby the liquid crystal material between the segment electrode a and the electrode X is continually driven by alternating current.

When a segment signal does not appear at the terminal 17Aa it is at level L, the transmission gate 37a therefore becomes conductive when the signal applied to the terminal 34 is at level H so that the segment electrode a is logical "0" as also is the electrode X. The voltage at the terminal 32 is applied to the segment electrode a and to the electrode X when the signal applied to the terminal 34 is level L because the transmission gate 36a is conductive. Therefore, no electric field exists between the segment electrode a and the electrode X so that the liquid crystal material therebetween is not driven.

The other segment electrodes b to g are operated in a similar manner. Further, the voltage of the terminal 32 namely, one of the voltages appearing at the terminals a₁, a₂, a₃, a₄ of the voltage level circuit 4 is selected by the switching circuit 6.

The liquid crystal display device 9, in this embodiment, may selectively have any one of four colours. Therefore, months, days of the month, hours and minutes are selectively displayed by the liquid crystal display device 9, and simultaneously with change of information displayed, the colour of the display changes. Thus the user can easily distinguish the information being displayed at any given instant.

It is possible to make the liquid crystal display device 9 display seconds by employing a further voltage level by the voltage level circuit 4. Further, it is possible to display months and days of the month simultaneously in the same colour or different colours by employing a liquid crystal display device having four alphanumeric display units, and similarly to display hours and minutes in the same or different colours, again by employing four alphanumeric display units. It will be appreciated that it is, therefore, easy to distinguish between a display of month and days of the month, and a display of hours and minutes.

In the place of the mechanical switch 7, it is possible to display cyclically the time signals by employing a signal obtained from a given dividing stage of the dividing circuit which forms part of the time keeping circuit 1.

WHAT WE CLAIM IS:—

1. A digital electronic timepiece comprising: a time signal pulse generating circuit; a time counting circuit for generating time signals corresponding to seconds, minutes, hours and date; a liquid crystal display means having retardation effect for displaying a digital time unit signal in different colours according to the drive voltage applied; a first switching circuit for selectively supplying different time unit signals from said time counting circuit to said display means for visual display thereby; a voltage level circuit for producing a plurality of different drive voltages

- for driving said liquid crystal display means; and a second switching circuit means coordinated with said first switching circuit means to supply from said voltage level circuit to said display means a selected drive voltage corresponding to a selected time unit signal to be displayed so that different time unit signals are distinguished from one another by being displayed in different colours.
- 10 2. A digital electronic timepiece as claimed in claim 1, in which said display means consists of means for displaying two digits.
- 15 3. A digital electronic timepiece as claimed in claim 1 or 2 including manually operable switch means for jointly controlling said first switching circuit means and said second switching circuit means.
- 20 4. A digital electronic timepiece as claimed in any preceding claim including a driving circuit for driving said display means, said driving circuit having inputs connected respectively to said first switching circuit means and said second switching circuit means and outputs connected to said display means.
5. A digital electronic timepiece as claimed in any preceding claim, in which said voltage level circuit comprises means for providing four different drive voltages.
6. A digital electronic timepiece as claimed in claim 4 or claim 5 when dependent thereon, in which said display means comprises segment electrodes and a figure electrode said driving circuit comprising means controlled by voltage pulses supplied by said time signal pulse generating circuit for supplying a selected drive voltage alternately to selected ones of said segment electrodes and said figure electrode to display a selected time signal in a selected colour.
7. A digital electronic timepiece substantially as herein described with reference to and as shown in the accompanying drawings.

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