

CLAIMS

1. A method for wireless communication, comprising:
transmitting, by a network node, a configuration for random access comprising a value indicative of a number of Zadoff-Chu, ZC, sequence roots, M , and a number of repetitions, N , if a difference between a first round-trip delay time between the network node and a first wireless device and a second round-trip delay time between the network node and a second wireless device is greater than a symbol time, T_{symbol} , that is a time duration of each ZC sequence of the M concatenated ZC sequences,
transmitting, by the network node, a cyclic shift configuration, if the difference between the first round-trip delay time and the second round-trip delay time is smaller than the symbol time, T_{symbol} ; and
receiving, from one or more wireless devices, one or more random access preambles based on the configuration, respectively,
wherein in case the configuration for random access comprises the values M and N the received random access preamble or each of the received random access preambles comprises M concatenated ZC sequences with different roots, and wherein each of the M concatenated ZC sequences is repeated based on N .
2. The method of claim 1, wherein the one or more random access preambles is received in a reception window with a size that is based on M and N , in case the configuration for random access comprises the values M and N .
3. The method of claim 1 or 2, wherein each ZC sequence has a fixed common cyclic shift in case the configuration for random access comprises the values M and N .
4. The method of claim 3, wherein a length of the random access preamble is $M \times N \times T_{\text{symbol}}$ in case the configuration for random access comprises the values M and N .
5. The method of claim 1 or 2, wherein a length of each ZC sequence of the M concatenated ZC sequences is 839 symbols or 139 symbols.

6. The method of any of claims 1 to 5, wherein the network node comprises a satellite.
7. A wireless communications apparatus comprising a processor and a memory, wherein the processor is configured to read code from the memory and implement a method recited in any of claims 1 to 6.
8. A computer program product comprising a computer-readable program medium code stored thereupon, the code, when executed by a processor, causing the processor to implement a method recited in any of claims 1 to 6.