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Description

Method for producing a multichip module and multichip module

The present invention relates to a method for producing a multichip module and a corresponding multichip module, and in particular to a method for producing a multichip system in a package.

In order to be able to provide complete semiconductor system solutions, it is necessary to be able to integrate different functional units within a component. For such integration, it is possible on the one hand to choose an SoC approach (system on chip) or on the other hand an SiP approach (system in a package). SiP solutions afford the advantage that, within a package, separate chips can in each case be individually optimized, tested and produced cost-effectively as functional units. In contrast, in the case of an SOC, all the functional units are integrated within a singular chip. What is problematic in the case of SiP solutions is that the individual chips within the package, preferably within a chip stack, have to be electrically conductively connected together among one another. In order to provide these electrically conductive connections between individual chips within a chip stack, it is known for a number of methods to be used. FIG. 16 illustrates two known embodiments.

In the upper illustration in accordance with FIG. 16, a first chip A is mechanically connected to a second chip C lying above it via an interposer B. The chips A, C are electrically contact-connected via bonding wires D within the package E. The package E can be connected to a printed circuit board (not illustrated) for example via solder balls F.

In the lower known configuration illustrated in

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accordance with FIG. 16, a semiconductor chip A is electrically connected to a chip C via solder balls F'. The chip C likewise has bonding wires D for rewiring and contact-connection of solder balls F within the package E. The package E can be electrically contact-connected externally via the solder balls F. The known configurations explained in accordance with FIG. 16 have poor electrical properties on account of large parasitic effects at high frequencies. Based on the high inductance and capacitance of the bonding wire, many connecting points and a lack of impedance matching.

A wiring via rewiring substrates or interposers e.g. in the form of a folded package is additionally known. Such an arrangement gives rise to long signal paths, however, which likewise result in poor electrical properties at high frequencies. What is more, such a known arrangement is associated with high substrate costs.

A thin-film rewiring via the edge of a chip previously embedded with polymer to a through-plating location is likewise known. At the through-plating location, electrically conductive plated-through holes are generated in the embedding polymer prior to the separation of a wafer. Such through-plating locations are provided, for example, by holes or openings filled with metallizations. The complex processing associated with high costs is disadvantageous in this case.

It is known, moreover, to provide plated-through holes within a chip, for example by means of through-Si-vias. In the course of the contact-connection through the chip, vias are etched into the chip in this case (dry etching, wet etching). These contact-connections are thereupon passivated with subsequent metallization of the entire via. The via is metallized by the walls being metallized and the via subsequently being filled

with a conductive material. This gives rise to the disadvantages that free areas have to be provided on the chip for through-plating, which necessitates an enlargement of the chip area. Moreover, the processing is complex and associated with high costs in this case as well.

Therefore, it is an object of the present invention to provide a method for producing a multichip module and a corresponding multichip module by means of which electrically conductive connections are generated from a chip plane to an overlying chip plane.

According to the invention, this object is achieved by means of the method for producing a multichip module as specified in Claim 1 and by means of the multichip module according to Claim 8.

The idea on which the present invention is based essentially consists in firstly providing a contact elevation and a rewiring device on the contact elevation, a chip subsequently being electrically connected to the rewiring device, whereupon embedding in an encapsulating device is effected. The contact elevation or the three-dimensional connecting element is preferably formed by a printed elevation made of a nonconductive material, such as silicone, polyurethane, polyimide, for example, or a conductive material, such as e.g. conductive adhesive, with fluid transitions to an underlying substrate, such as e.g. a sheet. Said substrate has the preferably metallic, patterned rewiring layer.

By means of the production method according to the invention and the multichip module according to the invention, a multiplicity of chips in a chip stack can advantageously be connected to one another in a simple and cost-effective manner. The use of cost-intensive rewiring substrates or disadvantageous bonding wires

can thus be avoided. Following the production method according to the invention, a high degree of parallelism is made possible in the production process since, by way of example, 12 inch substrates or rectangular substrates or else a reel-to-reel method can be used. Complex metallization and filling of contact holes is not necessary, just as little as vertical patterning after separation of the chip stack along chip edges.

In the present invention, the problems mentioned in the introduction are solved in particular by the provision of a method for producing a multichip module having the following steps: application of at least one contact elevation onto a substrate; application and patterning of a rewiring device onto the substrate and the at least one contact elevation with provision of a contact device on the at least one contact elevation; application of a semiconductor chip onto the substrate with electrical contact-connection of the rewiring device; application of an encapsulating device that is not electrically conductive onto the semiconductor chip, the substrate, the rewiring device and the at least one contact elevation, the contact device of the at least one contact elevation at least touching a first surface of the encapsulating device; and repetition at least once of at least the first two steps, the first surface of the encapsulating device serving as a substrate and the correspondingly produced rewiring device making electrical contact with the contact device of the at least one contact elevation of the underlying plane.

Advantageous developments and improvements of the respective subject matter of the invention are found in the subclaims.

In accordance with one preferred development, the at least one contact elevation is printed on or is applied

in an injection-molding step or a stamping step or a metering step.

In accordance with a further preferred development, a chip contact device is applied onto the rewiring device which is electrically contact-connected to the semiconductor chip.

In accordance with a further preferred development, the chip contact device is electrically conductively connected to the rewiring device by soldering or adhesive bonding with conductive adhesive or diffusion soldering or compression bonding.

In accordance with a further preferred development, the nonconductive encapsulating device is applied by printing or an injection-molding step or potting or spraying-on or spinning-on.

In accordance with a further preferred development, after the application of the nonconductive encapsulating device, the contact device on the at least one contact elevation is cleaned, preferably in a plasma or wet etching step.

In accordance with a further preferred development, besides semiconductor chips, provision is made of at least one passive component and/or a memory and/or an optical semiconductor device in the encapsulating device with electrical contact-connection to the rewiring device.

In accordance with a further preferred development, the rewiring device is applied by means of a sputtering or plating process and is subsequently patterned photolithographically, preferably by means of a wet etching step.

In accordance with a further preferred development, on

the multichip module, above a final encapsulating device, solder balls or contact elevations or contact areas are applied as a connection device, in each case preferably in a manner connected conductively to an underlying plane via a rewiring device.

In accordance with a further preferred development, a sheet is provided as the substrate.

In accordance with a further preferred development, the contact elevation has a nonconductive material, preferably silicone or polyimide or polyurethane, or a conductive material, preferably conductive adhesive.

In accordance with a further preferred development, the at least one contact elevation is bell-shaped and preferably has a transition with a small gradient between the substrate and the contact elevation.

In accordance with a further preferred development, a chip contact device is applied onto the rewiring device, and is electrically contact-connected to the semiconductor chip and the rewiring device.

In accordance with a further preferred development, the chip contact device is provided as a solder deposit or stud bump or fixed contact on the rewiring device.

In accordance with a further preferred development, the encapsulating device has a polymer.

In accordance with a further preferred development, at least two semiconductor chips in the multichip module face one another with their chip contacts.

In accordance with a further preferred development, the rewiring device is metallic and preferably has a soldering resist layer or a passivation in predetermined regions.

Exemplary embodiments of the invention are illustrated in the drawings and are explained in more detail in the description below.

In the figures:

FIGS 1 to 11 each show a diagrammatic cross-sectional view of successive steps in the production of a multichip module in accordance with an embodiment of the present invention;

FIGS 12 to 14 each show a diagrammatic cross section of a multichip module in accordance with a respective embodiment of the present invention;

FIG. 15 shows a diagrammatic plan view and a diagrammatic cross section of a multichip module for elucidating an embodiment of the present invention; and

FIG. 16 shows two known multichip modules.

In the figures, identical reference symbols designate identical or functionally identical component parts.

FIG. 1 illustrates a substrate 10, preferably a sheet, in cross section. In accordance with FIG. 2, at least one contact elevation 11 is applied thereto. The contact elevation 11 is made of a polymer, for example, which may be conductive, such as conductive adhesive, for example, or nonconductive, such as silicone, polyurethane, polyimide, for example. The application of the at least one contact elevation 11 is preferably effected in a printing operation or a metering operation or an injection-molding operation or a stamping step. The at least one contact elevation 11 is

preferably bell-shaped and has a small gradient in the transition from the substrate 10 to the contact elevation 11. In this connection, a small gradient is understood to be a gradient of less than 0.5.

In accordance with FIG. 3, a rewiring device 12 is applied and patterned onto the substrate 10 and the at least one contact elevation 11. In this case, the rewiring device 12 preferably has in each case a contact device 13 on a contact elevation 11. The contact device 13 on the contact elevation 11 is preferably obviated in the case of a contact elevation 11 made of a conductive material, the rewiring device 12 making electrical contact with the then conductive contact elevation 11. The rewiring device 12 is preferably sputtered on or plated electrochemically, patterned in a photolithographic process, preferably by means of a wet etching technique, and has a passivation or a soldering resist layer over predetermined sections (not illustrated).

In accordance with FIG. 4, a chip contact device 14 is thereupon applied, which is electrically conductively connected to the rewiring device 12. The cross sections in accordance with FIG. 3 to FIG. 11 in each case illustrate two strands of a rewiring device 12 that are electrically isolated from one another, i.e. an electrically conductive connection in the form of the rewiring device 12 is not provided between the chip contact devices 14 in accordance with FIG. 4 ff. The chip contact device 14 is preferably provided by applying a solder deposit or a conductive adhesive deposit or a stud bump.

In FIG. 5, a semiconductor chip 15 is applied, preferably adhesively bonded, onto the arrangement in accordance with FIG. 4, the chip contact device 14 being electrically conductively connected to chip contacts (not illustrated) of the semiconductor device

15. This presupposes a precise positioning of the semiconductor chip 15 on the substrate 10. The electrical contact-connection of the chip contacts (not illustrated) to the chip contact device 14 is preferably effected by means of a solder reflow or a pressure contact or by diffusion soldering or an adhesive bonding connection using a conductive adhesive.

In accordance with FIG. 6, an encapsulating device 16 is applied above the chip 15, the rewiring device 12, the at least one contact elevation and the substrate 10 in the form of a nonconductive polymer. The encapsulating device 16 is preferably applied by printing on or injection molding or spraying on or spinning on of a nonconductive material. In this case, the vertical extent of the encapsulating device 16 does not exceed the vertical extent of the at least one contact elevation 11, so that the contact device 13 on the contact elevation 11 or the contact elevation 11 itself touches at least one surface 16′ (covering area) of the encapsulating device 16. Preferably, the vertical extent of a contact elevation 11 projects above the vertical extent of the encapsulating device 16. In the case of the arrangement in accordance with FIG. 6, this is preferably followed by cleaning of the tips of the contact elevation 11 and in particular of the contact device 13 on the tips of the contact elevation 11, preferably in a plasma or wet etching step.

FIG. 7 shows the arrangement in accordance with FIG. 6 after contact elevations 11 have been applied onto the surface 16′ of the encapsulating device 16. The contact elevations 11 on the surface 16′ are arranged laterally adjacent to the uncovered contact devices 13 of the contact elevations 11 of the underlying plane. The contact elevations 11 on the surface 16′ are applied in the manner explained with reference to FIG. 2. This is

followed by application and patterning of a rewiring device 12 onto the surface 16′ of the encapsulating device 16 and the contact elevations 11 on the surface 16′ with the formation of contact devices 13 in accordance with FIG. 8. The rewiring device 12 is applied and patterned like the one explained with reference to FIG. 3. Contrary to the sectional illustration in accordance with FIG. 8, a conductor track of the rewiring device 12 on the surface 16′ that is led onto a contact elevation 11 on the surface 16′ and forms a contact device 13 on the tip is preferably not contact-connected to the contact device 13 on the contact elevation 11 of the underlying plane, but rather rewired with a laterally adjacent conductor track (not illustrated in the sectional illustration).

In accordance with FIG. 9, a chip contact device 14 is applied onto the arrangement in accordance with FIG. 8, which is preferably identical to the chip contact device 14 of the underlying plane.

FIG. 10 illustrates the arrangement according to FIG. 9, a second semiconductor chip 15 being applied onto the surface 16′ with contact-connection of the rewiring device 12, preferably via the chip contact device 14. The orientation and fixing of the second semiconductor chip 15 on the surface 16′ correspond to the operation described with reference to FIG. 5.

In accordance with FIG. 11, an encapsulating device 16 in accordance with FIG. 6 is likewise applied above the second semiconductor chip 15, the rewiring device 12, the contact elevation 11 in each case on the surface 16′.

FIG. 12 illustrates a cross section of a multichip module which, in comparison with FIG. 11, has two further semiconductor chips 15 in two further overlying planes. A multiplicity of contact elevations 17 are

applied onto a final surface 16' of a final encapsulating device 16. These connecting elements for contact-connection, for example to a printed circuit board or an interposer (not illustrated in either case), are preferably likewise provided in the form of a polymer elevation comprising a conductive or nonconductive material, as described with reference to FIG. 2. A rewiring device 18 is likewise provided on the surface 16' of the topmost encapsulating device 16, which rewiring device preferably also forms contact devices 19 on the tip of the contact elevations 17. The rewiring device 18 is electrically conductively connected to contact devices 13 on the contact elevations 11 of the underlying plane.

FIG. 13 shows an alternative embodiment of the present invention, in which two semiconductor chips 15 with chip contacts (not illustrated) that face one another are provided, which are in each case electrically conductively connected to a chip contact device 14. Contrary to the impression of the drawing in accordance with FIG. 13, the chip contact devices of the upper semiconductor chip 15 and of the lower semiconductor chip 15 are not directly electrically conductively connected to one another. This requires a modified production process.

A further embodiment in accordance with FIG. 14 has the chips that face one another in accordance with FIG. 13 and a further semiconductor chip 15 arranged thereabove. All further essential features correspond to the above explanations.

A cross section and an associated plan view for elucidating an embodiment of the present invention are illustrated diagrammatically with reference to FIG. 15. In this case, the sectional illustration corresponds to a section along the broken line ZZ'.

Although the present invention has been described above on the basis of preferred exemplary embodiments, it is not restricted thereto, but rather can be modified in diverse ways. Thus, in particular, other forms of the contact elevation produced are conceivable, for example as a bump, bead or with regard to the lateral and vertical extent. Moreover, the way of producing the contact elevation, in addition to the possibilities mentioned, is also possible by application, in particular adhesive bonding, of a preformed elevation.

In addition, it is possible to provide, instead of the contact elevations 17 with contact devices 19 on the tip thereof, other contact elements for the electrical connection to further electrical or electronic components, such as, for example, contact areas or else solder balls that are contact-connected via a rewiring device 18. Any desired configurations are possible with regard to the stack height and fashioning of the chips or the chip arrangement, so that, by way of example, different chip sizes or else chips are provided next to one another within a plane in a multichip module according to the invention. Furthermore, relative sizes reproduced in the drawings are to be regarded as merely by way of example.

List of reference symbols

10	Substrate, preferably sheet
11	Contact elevation
12	Rewiring device
13	Contact device on contact elevation
14	Chip contact device
15	Semiconductor chip
16	Encapsulating device
16'	Surface of the encapsulating device
17	Contact elevation
18	Rewiring device
19	Contact device on contact elevation

A	Chip
B	Interposer substrate
C	Chip
D	Bonding wire
E	Chip package
F, F'	Solder ball

Patent Claims

1. Method for producing a multichip module having the following steps:

(a) application of at least one contact elevation (11) onto a substrate (10);

(b) application and patterning of a rewiring device (12) onto the substrate (10) and the at least one contact elevation (11) with provision of a contact device (13) on the at least one contact elevation (11);

(c) application of a semiconductor chip (15) onto the substrate (10) with electrical contact-connection of the rewiring device (12);

(d) application of an encapsulating device (16) that is not electrically conductive onto the semiconductor chip (15), the substrate (10), the rewiring device (12) and the at least one contact elevation (11), the contact device (13) on the at least one contact elevation (11) at least touching a first surface (16') of the encapsulating device (16); and

(e) repetition at least once of at least steps (a) and (b), the first surface (16') of the encapsulating device (16) serving as a substrate and the correspondingly produced rewiring device (12) making electrical contact with the contact device (13) of the at least one contact elevation (11) of the underlying plane.

2. Method according to Claim 1,
characterized
in that the at least one contact elevation (11) is printed on or is applied in an injection-molding step or a stamping step or a metering step.

3. Method according to Claim 1 or 2, characterized in that between steps (b) and (c), a chip contact device (14) is applied onto the rewiring device (12) which is electrically contact-connected to the semiconductor chip (15) in step (c).

4. Method according to Claim 3, characterized in that the chip contact device (14) is electrically conductively connected to the rewiring device (12) by soldering or adhesive bonding with conductive adhesive or diffusion soldering or compression bonding.

5. Method according to one of the preceding claims, characterized in that the nonconductive encapsulating device (16) is applied by printing or an injection-molding step or potting or spraying-on or spinning-on.

6. Method according to one of the preceding claims, characterized in that, after the application of the nonconductive encapsulating device (16) in accordance with step (d), the contact device (13) on the at least one contact elevation (11) is cleaned, preferably in a plasma or wet etching step.

7. Method according to one of the preceding claims, characterized in that, besides semiconductor chips (15), provision is made of at least one passive component and/or a memory and/or an optical semiconductor device in the encapsulating device (16) with electrical contact-connection to the rewiring device (12).

8. Method according to one of the preceding claims, characterized in that the rewiring device (12) is applied by means of

a sputtering or plating process and is subsequently patterned photolithographically, preferably by means of a wet etching step.

9. Method according to one of the preceding claims, characterized
in that, on the multichip module, above a final encapsulating device (16), solder balls or contact elevations (17) or contact areas are applied as a connection device, in each case in a manner connected conductively to an underlying plane via a rewiring device (18).

10. Multichip module having:

(a) at least one contact elevation (11) on a substrate (10);

(b) a rewiring device (12) on the substrate (10) and the at least one contact elevation (11) with provision of a contact device (13) on the at least one contact elevation (11);

(c) a semiconductor chip (15) on the substrate (10) with electrical contact-connection of the rewiring device (12);

(d) an encapsulating device (16) that is not electrically conductive on the semiconductor chip (15), the substrate (10), the rewiring device (12) and the at least one contact elevation (11), the contact device (13) of the at least one contact elevation (11) at least touching a first surface (16') of the encapsulating device (16); and

(e) repetition at least once of at least features (a) and (b), the first surface (16') of the encapsulating layer (16) serving as a substrate and the corresponding rewiring device (12) making electrical contact with the

contact device (13) of the at least one contact elevation (11) of the underlying plane.

11. Multichip module according to Claim 10, characterized in that a sheet is provided as the substrate (10).

12. Multichip module according to Claim 10 or 11, characterized in that the contact elevation (11) has a nonconductive material, preferably silicone or polyimide or polyurethane, or a conductive material, preferably conductive adhesive.

13. Multichip module according to Claim 12, characterized in that the at least one contact elevation (11) is bell-shaped and preferably has a transition with a small gradient between the substrate (10) and the contact elevation (11).

14. Multichip module according to one of Claims 10 to 13, characterized in that a chip contact device (14) is applied onto the rewiring device (12), and is electrically contact-connected to the semiconductor chip (15) and the rewiring device (12).

15. Multichip module according to Claim 14, characterized in that the chip contact device (14) is provided as a solder deposit or stud bump or conductive adhesive deposit on the rewiring device (12).

16. Multichip module according to one of Claims 10 to 15, characterized in that the encapsulating device (16) has a polymer.

17. Multichip module according to one of Claims 10 to 16,
characterized
in that at least two semiconductor chips (15) in the multichip module face one another with their chip contacts.

18. Multichip module according to one of Claims 10 to 17,
characterized in that the rewiring device (12) is metallic and preferably has a soldering resist layer or a passivation in predetermined regions.