159159

THERMAL STABILITY IMPROVEMENT OF $CoSi_2$ FILM BY STUFFING IN TITANIUM

BACKGROUND OF THE INVENTION

G00002

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of forming a thermally stable cobalt silicide film in the fabrication of integrated circuits.

(2) Description of the Prior Art

Cobalt disilicide ($CoSi_2$) is a preferred salicide technology as CMOS device sizes shrink to 0.18 μm and beyond because of its good performance with small polysilicon and active area line widths. Cobalt disilicide also has been widely accepted in deep sub-micron devices to reduce the contact resistance. As device scales shrink further and molecular processes evolve, the requirement for cobalt disilicide film properties becomes more stringent. One of the concerns over the cobalt disilicide ($CoSi_2$) film properties is its thermal stability. It is known that the thermal stability of $CoSi_2$ is thickness dependent. That is, the thinner the $CoSi_2$ film, the more thermally unstable it becomes. The sheet resistance of the thin $CoSi_2$ film could

be increased significantly when it experiences a thermal stress in subsequent processing. On the other hand, for shallow junctions, the $CoSi_2$ thickness must be decreased. Thus, the $CoSi_2$ film thermal stability for thin films must be improved.

A number of patents disclose methods of forming $CoSi_2$. U.S. Patent 6,022,457 to Huang et al discloses cleaning the native oxide layer off the silicon substrate, then depositing a titanium layer under the cobalt layer. A silicon layer may be deposited over the titanium layer and under the cobalt layer. A RTA process forms $CoSi_2$. U.S. Patent 6,083,817 to Nogami et al teaches a tungsten nitride capping layer over the cobalt layer. U.S. Patent 6,025,267 to Pey et al discloses a titanium nitride layer over the cobalt. U.S. Patent 5,869,396 to Pan et al shows a method of forming cobalt disilicide.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of fabricating a cobalt disilicide film in the fabrication of an integrated circuit.

A further object of the invention is to provide a method of fabricating a thermally stable cobalt disilicide film in the fabrication of an integrated circuit.

Yet another object is to provide a method of forming a thermally stable cobalt disilicide film by using a titanium stuffing technique.

In accordance with the objects of the invention a method for forming a thermally stable cobalt disilicide film in the fabrication of an integrated circuit is achieved. A semiconductor substrate is provided having silicon regions to be silicided. A cobalt layer is deposited overlying the silicon regions to be silicided. A capping layer is deposited overlying the cobalt layer. The substrate is subjected to a first rapid thermal anneal whereby the cobalt is transformed to cobalt monosilicide where it overlies the silicon regions and wherein the cobalt not overlying the silicon regions is unreacted. The unreacted cobalt layer and the capping layer are removed. A titanium layer is deposited overlying the cobalt monosilicide layer. Thereafter the substrate is subjected to a second rapid thermal anneal whereby the cobalt monosilicide is transformed to cobalt disilicide. During this transformation, some titanium atoms diffuse into and are incorporated into the

cobalt disilicide film. The titanium layer is removed to complete formation of a thermally stable cobalt disilicide film in the manufacture of an integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 7 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

Fig. 8 schematically illustrates in cross-sectional representation a completed integrated circuit fabricated according to a preferred embodiment of the present invention.

Fig. 9 graphically illustrates both resistance and non-uniformity as functions of thermal cycles for samples made according to a standard process and according to the process of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The process of the present invention can be used in any application in which it is desired to form a cobalt disilicide film overlying a silicon region. The process of the invention will be described for the application in which $CoSi_2$ is formed overlying a gate electrode and source and drain regions. It is to be understood that the invention is not limited to the application so illustrated.

Referring now more particularly to Fig. 1, there is shown an illustration of a portion of a partially completed integrated circuit. The semiconductor substrate 10 is preferably composed of silicon having a (100) crystallographic orientation. Gate electrode 16 and source and drain regions 20 are formed in and on the semiconductor substrate as is conventional in the art. For example, gate electrode 16 has been formed overlying a gate oxide layer 14. Sidewall spacers, such as silicon oxide, 18 are formed on the gate. Source and drain regions are n-type or p-type, depending on the type of device to be fabricated.

As shown in Fig. 2, a layer of cobalt 22 is sputter deposited over the surface of the substrate and the

gate electrode to a thickness of between about 50 and 150 Angstroms. Next, a capping layer of titanium or titanium nitride 24 is deposited over the cobalt layer to a thickness of between about 50 and 200 Angstroms. The titanium or titanium nitride capping layer will prevent any foreign contaminant invasion during the first annealing process.

Now, the wafer is subjected to a first rapid thermal annealing (RTA) at a temperature of between about 450 and 650 °C for 15 to 90 seconds. This annealing will form cobalt monosilicide (CoSi) 26 over the gate electrode and over the source and drain regions, as shown in Fig. 3. Layer 28 contains unreacted cobalt and titanium or titanium nitride residue.

The unreacted cobalt and titanium residue layer is etched back from the wafer surface, leaving the CoSi film 26 over the gate electrode 16 and the source and drain regions 20, as shown in Fig. 4.

Now, in a key step, a layer of titanium 30 is deposited over the silicided gate electrode and source and drain regions to a thickness of between about 50 and 200 Angstroms, as shown in Fig. 5.

To complete the low resistance cobalt silicide film formation, the wafer is subjected to a second RTA, this time at a temperature of between about 700 and 900 °C, to transform the cobalt monosilicide (CoSi) to cobalt disilicide ($CoSi_2$) 32, as illustrated in Fig. 6. During this RTA, some of the titanium atoms from the titanium layer 30 will diffuse into the cobalt disilicide film 32, thus increasing the thermal stability of the cobalt disilicide.

The titanium residue 34 remains overlying the $CoSi_2$ layer 32. A second etchback removes the titanium residue, leaving the completed silicided gate and source and drain regions, as shown in Fig. 7.

Standard backend processing continues as is conventional to complete the integrated circuit. For example, Fig. 8 shows a thick dielectric layer 36 covering the silicided gate and source and drain regions. Electrical connections may be made, for example, to one of the silicided source/drain regions 20 by metal contact 40, as shown.

EXAMPLE

The following Example is given to show the important features of the invention and to aid in the

understanding thereof. Variations may be made by one skilled in the art without departing from the spirit and scope of the invention.

The process of the present invention has been implemented. Experiments were performed in which cobalt disilicide films were formed using the process of the invention in which a first titanium overlayer was formed over a cobalt layer, a first RTA was performed and the unreacted residue was removed, a second titanium layer of 50 to 200 Angstroms was formed over the cobalt monosilicide, and a second RTA was performed followed by removal of the titanium residue. A control was made using a standard process in which a first titanium overlayer was formed over a cobalt layer, a first RTA was performed and the unreacted residue was removed and a second RTA was performed.

Sheet resistance (Rs) and its non-uniformity (RsU) increments were measured for each of the samples after thermally annealing the samples ten times at 850 °C for 30 seconds (to provide thermal stress). For the standard process, the change in sheet resistance was an increase of about 33.6% while the change in sheet resistance non-uniformity was an increase of about 125.9%. For the process of the present invention, the change in sheet resistance was

an increase of about 4.3% and the change in sheet resistance non-uniformity was an increase of about 3.7%. Because of the titanium stuffing process of the present invention, film sheet resistance is not affected significantly.

Fig. 9 graphically illustrates the results of the thermal stress testing described above. Thermal annealing cycle numbers are shown on the horizontal axis. Line 91 shows the resistance (on the lefthand axis) of the sample made by the standard process as thermal cycles increase. Line 92 shows the resistance of the sample made by the process of the invention.

Line 95 shows the non-uniformity (on the righthand axis) of the sample made by the standard process as thermal cycles increase. Line 96 shows the non-uniformity of the sample made by the process of the invention.

The process of the invention provides an effective method of forming $CoSi_2$ especially for shallow junctions and small feature sizes by use of a titanium layer over the cobalt monosilicide during the second RTA that forms cobalt disilicide. This titanium layer provides a titanium atom source which diffuses into the cobalt disilicide film thereby forming a cobalt disilicide having greater thermal

stability and, therefore, much lower sheet resistance than conventional cobalt disilicide layers. The process of the invention is especially useful for thin silicide layers required for shallow junctions.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of fabricating a cobalt disilicide film in the manufacture of an integrated circuit comprising:

providing a semiconductor substrate having silicon regions to be silicided;

depositing a cobalt layer overlying said silicon regions to be silicided;

depositing a capping layer overlying said cobalt layer;

subjecting said substrate to a first rapid thermal anneal whereby said cobalt is transformed to cobalt monosilicide where it overlies said silicon regions and wherein said cobalt not overlying said silicon regions is unreacted;

removing said unreacted cobalt layer and said capping layer;

depositing a titanium layer overlying said cobalt monosilicide layer;

thereafter subjecting said substrate to a second rapid thermal anneal whereby said cobalt monosilicide is transformed to cobalt disilicide; and

removing said titanium layer to complete formation of said cobalt disilicide film in the manufacture of said integrated circuit.

2. The method according to Claim 1 wherein said silicon regions to be silicided comprise gate electrodes and associated source and drain regions.

3. The method according to Claim 1 wherein said cobalt layer is sputter deposited to a thickness of between about 50 and 150 Angstroms.

4. The method according to Claim 1 wherein said capping layer comprises titanium sputter deposited to a thickness of between about 50 and 200 Angstroms.

5. The method according to Claim 1 wherein said capping layer comprises titanium nitride sputter deposited to a thickness of between about 50 and 200 Angstroms.

6. The method according to Claim 1 wherein said first rapid thermal anneal is performed at a temperature of between about 450 and 650 °C.

7. The method according to Claim 1 wherein said titanium layer is sputter deposited to a thickness of between about 50 and 200 Angstroms.

8. The method according to Claim 1 wherein said second rapid thermal anneal is performed at a temperature of between about 700 and 900 °C.

9. A method of fabricating a cobalt disilicide film in the manufacture of an integrated circuit comprising:

providing a semiconductor substrate having silicon regions to be silicided;

depositing a cobalt layer overlying said silicon regions to be silicided wherein said cobalt layer can be as thin as 50 Angstroms;

depositing a capping layer overlying said cobalt layer;

subjecting said substrate to a first rapid thermal anneal whereby said cobalt is transformed to cobalt monosilicide where it overlies said silicon regions and wherein said cobalt not overlying said silicon regions is unreacted;

removing said unreacted cobalt layer and said capping layer;

depositing a titanium layer overlying said cobalt monosilicide layer;

thereafter subjecting said substrate to a second rapid thermal anneal whereby said cobalt monosilicide is transformed to cobalt disilicide; and

removing said titanium layer to complete formation of said cobalt disilicide film in the manufacture of said integrated circuit.

10. The method according to Claim 9 wherein said silicon regions to be silicided comprise gate electrodes and associated source and drain regions.

11. The method according to Claim 9 wherein said cobalt layer is sputter deposited to a thickness of between about 50 and 150 Angstroms.

12. The method according to Claim 9 wherein said capping layer comprises titanium sputter deposited to a thickness of between about 50 and 200 Angstroms.

13. The method according to Claim 9 wherein said capping layer comprises titanium nitride sputter deposited to a thickness of between about 50 and 200 Angstroms.

14. The method according to Claim 9 wherein said first rapid thermal anneal is performed at a temperature of between about 450 and 650 °C.

15. The method according to Claim 9 wherein said titanium layer is sputter deposited to a thickness of between about 50 and 200 Angstroms.

16. The method according to Claim 9 wherein said second rapid thermal anneal is performed at a temperature of between about 700 and 900 °C.

17. A method of fabricating a cobalt disilicide film in the manufacture of an integrated circuit comprising:

providing a semiconductor substrate having silicon regions to be silicided;

depositing a cobalt layer overlying said silicon regions to be silicided wherein said cobalt layer can be as thin as 50 Angstroms;

depositing a capping layer overlying said cobalt layer;

subjecting said substrate to a first rapid thermal anneal whereby said cobalt is transformed to cobalt monosilicide where it overlies said silicon regions and wherein said cobalt not overlying said silicon regions is unreacted;

removing said unreacted cobalt layer and said capping layer;

depositing a titanium layer overlying said cobalt

monosilicide layer;

thereafter subjecting said substrate to a second rapid thermal anneal whereby said cobalt monosilicide is transformed to cobalt disilicide wherein titanium atoms from said titanium layer diffuse into said cobalt disilicide thereby increasing thermal stability of said cobalt disilicide; and

removing said titanium layer to complete formation of said cobalt disilicide film in the manufacture of said integrated circuit.

18. The method according to Claim 17 wherein said silicon regions to be silicided comprise gate electrodes and associated source and drain regions.

19. The method according to Claim 17 wherein said cobalt layer is sputter deposited to a thickness of between about 50 and 150 Angstroms.

20. The method according to Claim 17 wherein said capping layer comprises titanium sputter deposited to a thickness of between about 50 and 200 Angstroms.

21. The method according to Claim 17 wherein said capping layer comprises titanium nitride sputter

deposited to a thickness of between about 50 and 200 Angstroms.

22. The method according to Claim 17 wherein said first rapid thermal anneal is performed at a temperature of between about 450 and 650 °C.

23. The method according to Claim 17 wherein said titanium layer is sputter deposited to a thickness of between about 50 and 200 Angstroms.

24. The method according to Claim 17 wherein said second rapid thermal anneal is performed at a temperature of between about 700 and 900 °C.