1343 173

PATENT SPECIFICATION (11) 1343 173

(21) Application No. 40961/71 (22) Filed 2 Sept. 1971
(31) Convention Application No. 69651 (32) Filed 4 Sept. 1970 in
(33) United States of America (US)
(44) Complete Specification published 9 Jan. 1974
(51) International Classification H01L 10/00//15/00
(52) Index at acceptance
H1K 211 216 21Y 235 238 243 244 248 26X 312 413 41Y 422 42X 441 458 459 469 482 483 486 491 511 51Y 520 530 543 54Y 55Y 563 578 581 591 59Y 611 618 61Y 650 65X

(19)



(54) SEMICONDUCTOR APPARATUS FOR SELECTIVELY MOVING ELECTRICAL CHARGES

(71) We, GENERAL ELECTRIC COMPANY, a corporation organized and existing under the laws of the State of New York, United States of America, residing at 1, River Road, Schenectady 12035, State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to conductor-insulator-semiconductor (CIS) devices and to apparatus embodying such devices for storage and transfer of electrical charges.

Basically, a CIS device can provide storage of electrical charges by the formation of depletion regions in the semiconductor underlying the conductor member. The electrical charges to be stored are generated either within the semiconductor itself in response to electromagnetic radiation or through injecting electrodes, for example.

In some information storage and processing systems it is often desirable to selectively move certain stored information from one storage location to another storage location while leaving other information unaffected. For example, a particular digital word stored among a group of words may be temporarily transferred from a memory to a binary adder for arithmetic processing, for example, and then the output of the binary adder returned to the memory. Alternately, information may be removed from a specific storage location so that other information may be stored temporarily at this location, then subsequently removed and the first information returned again to this location. In the case of analog information, for example, it is often desirable to selectively transfer certain groups of information sequentially.

According to the present invention there is provided a conductor-insulator-semiconductor device comprising: a substrate of semiconductor material, an insulator layer which overlies a major surface of said substrate and which is formed to present a plurality of cellules communicating with a common channel, a conductor member overlying said cellules, means for causing storage of electrical charges in the surface adjacent portions of said substrate substantially underlying said cellules, and means for transferring selected electrical charges between the surface-adjacent portions of said substrate underlying said cellules and said channel.

Briefly, in accord with one embodiment of the invention, electrical charges are stored and transferred along the surface-adjacent portions of a semiconductor substrate. This is achieved by providing a conductor-insulator-semiconductor storage and transfer device including an array of cellules formed in an insulator layer overlying the semiconductor substrate. The cellules may, for example, be arranged in rows and columns with a hold line insulatingly overlying each row of cellules and a charge transfer channel interconnected with each row of cellules. In one mode of operation, electrical charges are stored in potential wells formed in the surface-adjacent portions of the semiconductor substrate underlying the cellulus by the application of a semiconductor depletion region forming electric potential to the hold lines. The potential wells are made sufficiently deep so that the charges stored therein are substantially unaffected by the electric field associated with a network of charge transfer lines insulatingly overlying the hold lines and the transfer channels. By controllably removing the electric potential from a selected hold line however, the deep potential wells are no longer present and the electric charges stored under that hold line are now influenced by the electric field from the charge transfer lines. Under this influence, the charges are transferred to the row-associated charge transfer channel and from there to a bi-directional send-receive device, for example, for use elsewherein the processing system. In another

mode of operation, electrical charges are introduced into the charge transfer channel from a bidirectional send-receive device. These charges, under the influence of the electric field from the charge transfer lines, are brought to the desired storage location and are stored there by the application of an electric potential to the hold line.

The stored charges within the array may be representative of digital or analog signals transferred to the array through the charge transfer channels or generated within the array in response to electromagnetic radiation, for example, wherein the stored charges are representative of the incident radiation on the semiconductor substrate.

The novel features believed characteristic of the present invention are set forth in the appended claims. The invention itself, together with further objects and advantages thereof may best be understood by reference to the following detailed description of embodiments thereof taken in connection with the appended drawings in which:

FIGURE 1 is a partial plan view of a conductor-insulator-semiconductor array of storage device including apparatus for transferring selected electrical charges from one location to another;

FIGURE 2 is a partial cross-sectional view of the embodiment illustrated in FIGURE 2 taken along the line 2—2;

FIGURE 3 is a partial cross-sectional view of the embodiment illustrated in FIGURE 2 taken along the lines 3—3; and

FIGURE 4 is a schematic illustration of a solid state addressable electro-optical converter in accord with another embodiment of our invention.

FIGURE 1 illustrates, by way of example, an embodiment of our present invention as a portion of a two-dimensional solid state addressable, storage and transfer apparatus 11 comprising a conductor-insulator-semiconductor (CIS) structure. Basically, the CIS structure includes a substrate of semiconductor material 12 of substantially one electrical conductivity type, such as n-type silicon, for example, with an insulator layer 13 formed thereover. The insulator layer may, for example, be silicon dioxide, silicon nitride, silicon oxynitride, or combinations thereof. The insulator layer 13 includes a plurality of cellules 14 through 18, for example, arranged in a row with similar rows of cellules adjacent thereto. Each cellule is formed in the insulator layer as a region of thinner insulator material than the surrounding walls of the cellule. The formation of the cellules may, for example, be provided by selective masking and etching of the insulator material by techniques well known to those skilled in the art. Each row of cellules is separated from the next adjacent row of cellules by a channel formed in the insulating layer 13. FIGURE 1 illustrates these channels by the numerals 20 and 21. FIGURE 1 also illustrates openings 14a through 18a along the side walls of each cellule 14 through 18, respectively, which openings interconnect the cellules with the channel 20. The cellules of the next adjacent row have similar openings which interconnect those cellules with the channel 21. The channels 20 and 21, along with the openings in the side walls of each cellule may, for example, be formed at substantially the same time as the cellules are formed. Each channel and interconnecting opening between the cellules and the channels are conveniently of the same depth in the insulator layer so that the cellules, channels and interconnecting openings may all be formed at the same time.

In accord with the simplified embodiment of our invention illustrated in FIGURE 1, the CIS structure is completed by providing a conductor member 22 which overlies the cellules of row 1 and functions as a charge "hold line". A similar conductor member 23 overlies the cellules of row 2 and yet a third conductor member 24 overlies the cellules of row 3. The conductor members 22, 23 and 24 may, for example, be formed by depositing a continuous conductive material over the insulator layer and then appropriately masking and etching this layer to form the conductor members 22, 23 and 24. Conductive materials such as molybdenum, tungsten, tantalum, aluminum, gold, silver, platinum, silicon, germanium, or any of the other numerous non-reactive, conducting and semiconducting materials may advantageously be employed in practising the present invention.

The storage of electrical charges within the CIS structure illustrated in FIGURE 1 can be understood by those skilled in the art from the following description. A semiconductor material of n-type silicon, for example, is covered with an insulator layer of pyrolytically grown silicon dioxide having a thickness of approximately 10,000 Ångstroms. Cellular regions are etched in the silicon dioxide to a depth of approximately 9,000 Å to produce a silicon dioxide thickness of about 1,000 Å over the silicon in the cellular regions and the channel regions. Depletion regions are formed in those portions of the semiconductor substrate underlying the cellule while no depletion regions are formed elsewhere by the selective application of depletion region forming voltages to the conductor members 22, 23 and 24. For example, with the aforementioned insulator thicknesses, a 10-volt potential applied between the conductor member 22 and the semiconductor material 12 produces depletion regions only in those portions of the semiconductor substrate underlying the cellules 14 through 18. Those skilled in the art can appreciate that

the effective depth of the depletion region can be altered by varying the magnitude of the depletion region forming voltage or the thickness of the insulator layer. Further, by proper choice of the semiconductor material 11 the rate of arrival of minority carriers due to tunneling and avalanche multiplication at the surface of the semiconductor substrate can be rendered negligible for the storage times involved. Since the depletion regions also collect minority carriers existing in the semiconductor substrate due to normal thermal generation-recombination processes, the storage time in the depletion region is selected so that the effect of minority carriers arriving at the surface of the semiconductor due to thermal generation produces negligible effects. For the case of silicon, for example, at room temperatures, storage time intervals in the order of milliseconds and longer may be achieved before equilibrium through thermal generation is reached for the depletion region depths employed herein. Therefore, by insulring that no other source of minority carriers is present, after forming the depletion regions and removing or isolating the applied electric potential from the conductor members 22, 23 and 24, minority carriers may be controllably generated in response to electromagnetic radiation, for example, as shown by electromagnetic radiation rays 19. Alternately, minority carriers may be injected into the semiconductor by a P-N junction or a point contact, if desired.

When electromagnetic radiation, in the form of rays or images, for example, impinges on the semiconductor material 12, minority carriers are generated therein in proportional response to the radiation flux intensity. These minority carriers are swept to the semiconductor surface in response to the depletion region forming field and stored within the depletion regions underlying the cellules 14 through 18. For time intervals shorter than the surface equilibrium time, the amount of charge stored in each of the depletion regions is a direct measure of the integrated local radiation flux in the vicinity of the depletion region.

The depletion regions formed under the cellules as a result of the voltage potential applied to the hold lines are hereafter called "potential wells" since they are depletion regions at the semiconductor surface which, as stated above, have the ability to store minority carriers. The term "potential well" is also used to distinguish depletion regions which store electrical charges for selectively variable times from those which are used to transfer electrical charges and only provide temporary storage.

In accord with one of the novel features of our present invention, electrical charges introduced into potential wells by electromagnetic radiation, a P-N junction, a point contact of the launch-receive devices more fully disclosed in our concurrently filed application No. 40962/71 (Serial No. 1,343,174), for example, can be transferred from their respective potential wells to a transfer channel and from there to an output device while holding or continuing to store all other electric charges. In accord with yet another feature of our invention, the transfer of all selected charges is achieved by a single group of continuously clocking transfer signals which, however, are only able to transfer the selected electric charges with substantially no effect on other electric charges stored in the non-selected potential wells. These and other novel features of our invention are appreciated, for example, by the following description taken in connection with the accompanying drawing.

In FIGURE 1, a plurality of transfer lines 25—29 and 31—35 are illustrated as insulatingly disposed over the cellules and charge transfer channels. These transfer lines are positioned substantially orthogonal to the conductor members 22, 23 and 24. The overlapping relationship of these transfer lines is more clearly illustrated in FIGURE 2 which is a cross-sectional view taken along the lines 2—2 of FIGURE 1. In FIGURE 2, a first group of transfer lines includes members 25 through 29 and a second group of transfer lines includes members 31 through 35. Each member of the first group of members insulatingly overlies the cellules, the charge transfer channels and the interconnecting opening therebetween for a single column of cellules. As also illustrated in the drawing, each member 31 through 35 insulatingly overlaps adjacent members of the first group.

FIGURE 3, a cross-sectional view taken along the lines 3—3 of FIGURE 1, illustrates a portion of the charge transfer channel 21 with the overlapping charge transfer lines. FIGURE 3 also illustrates a P-N junction 40 formed in the semiconductor substrate 12. The P-N junction 40 may, for example, be provided by diffusion through an aperture in the inslator layer 13 which may subsequently be used to make contact to the diffused region, such as is illustrated by contact 41. As will be described more fully below, the P-N junction 40 may be used as a bi-directional send-receive device; that is, it may be used to introduce electrical charges into the semiconductor substrate or to remove charges therefrom.

The operation of the storage and transfer apparatus illustrated in FIGURES 1 through 3 can be understood by considering the sequence of events which occur in one mode of operation. For example, assume that an optical image is focused on the semiconductor substrate 12. Depending upon the intensity of the light signals striking the semiconductor material, a proportionate number of

minority carriers are generated. With the application of depletion region forming voltages, V_1, V_2 and V_3, for example, to conductor members 22, 23 and 24, respectively, the minority carriers generated by the incident light signals are collected in the potential wells underlying the cellules near the surface of the semiconductor material. As the light signals continue to impinge on the semiconductor material, the potential wells continue to accept minority carriers and provide integration of the light signals. After a suitable period of time, the electrical charges stored in the potential wells may be selectively removed from these regions and transferred to external circuitry through the P-N junction 40, for example.

The transfer of electrical charges is achieved by applying clock signals or transfer signals to the transfer lines 25 through 29 and 31 through 35 and by removing the depletion region forming voltage from one of the hold lines 22, 23 or 24. The transfer signals may, for example, comprise two signals of substantially the same frequency and waveshape but shifted in time by one-half the period and switching between two different voltage levels. If the first of these voltage signals is ϕ_1 and the second is ϕ_2, then by connecting these voltage signals to the transfer lines in the manner illustrated in FIGURES 1 and 3 of the drawing, surface charges may be transferred from one location to another on the semiconductor substrate. The magnitude of the voltage signals ϕ_1 and ϕ_2 is selected so that depletion regions are formed within the channel regions 20 and 21 and the openings between the channels and the cellules but not in regions where the insulator layer is substantially thicker than in the channel regions. Additionally, the depth of the potential well depletion region formed under each cellule is adjusted so that with a maximum electrical charge stored therein, no substantial change in charge is effected by the application of the transfer signals to the overlying transfer lines. In other words, the depletion region forming voltages when applied to conductor members 22, 23 and 24, hold or store the electrical charges in sufficiently deep potential wells that the charges are substantially unaffected by the presence of the shallower depletion regions underlying the transfer lines. However, when a depletion region forming voltage is removed from a hold line, the deep potential wells are no longer present and the electric charges stored under that hold line are now influenced by the electric field from the charge transfer lines. Under this influence, the electric charges are transferred to the row-associated charge transfer channel and from there to a receive device such as a P-N junction, for example.

The release or "read-out" of electric charges from selected locations on the semiconductor substrate can be understood by considering the following example. Assume that read-out of the electric charges stored in row one is desired. By reducing or removing the depletion region forming voltage V_1 from the hold line conductor member 22 while maintaining voltages V_2 and V_3 on hold line conductor members 23 and 24, the electric charges stored within the potential wells underlying the conductor member 22 are no longer under the influence of the hold line electric field, but are now influenced by the electric fields from the charge transfer lines. By synchronizing the removal of the voltage from member 22 with the application of transfer signals to transfer lines 25, 27 and 28, for example, the released charges flow into the row-associated charge transfer channel 20 through the interconnecting openings 14a—18a and then along the semiconductor surface underlying the charge transfer channel 20 to the P-N junction 40. The transfer of electrical charges along the channel 20 is provided by the transfer signals ϕ_1 and ϕ_2 which, in switching from one voltage level to another, sequentially move the electric fields and hence the electric charges along the transfer channel.

During the time interval that the electric charges are transferred from row one along the charge transfer channel, the other rows are still holding or storing their electric charges. In fact, if the electric charges are formed from the generation of minority carriers by incident electromagnetic radiation, these other rows continue to store and integrate the incident radiation. After read-out of the information from one row, the depletion region forming voltage may again be applied to conductor member 22 and the depletion region forming voltage removed from conductor 23, for example. The electrical charges underlying this conductor are then transferred to the row-associated charge transfer channel 21 and the electric charges are moved along this channel by similar transfer signals in substantially the same manner as described above with respect to row one. This mode of read-out is continued until all rows are scanned and then the sequence begins again.

The read-out of stored electrical charges on a row-by-row basis produces a voltage signal representative of the stored electrical charges. In the case where the charges are produced by electromagnetic radiation incident on the semiconductor substrate, the voltage signal is substantially similar to a video signal produced from an image converter. By appropriately synchronizing the read-out of stored electric charges with a suitable cathode ray tube display, for example, the stored electric charges can be displayed thereon. Those skilled in the art can readily appreciate that such a storage and transfer

device which does not require the use of a scanning electron beam has great commercial utility.

A particularly useful embodiment of our invention is illustrated in FIGURE 4 wherein a two-dimensional optical image converter 50 comprising an integrated array of CIS storage elements 51 are arranged in an "X-Y Pattern" on a semiconductor substrate. The storage elements and the transfer channels are substantially similar to those described above and operate in substantially the same manner. The optical image converter 50 further comprises row select generator circuitry 52 which may, for example, be fabricated on the semiconductor substrate as integrated circuitry and include the necessary circuitry to scan each row and provide the depletion region forming voltages to the appropriate conductor member hold lines during the read-in times and to selectively remove these voltages during the read-out times. The optical image converter 50 also includes a transfer control generator 53, which may, for example, includes a two- or three-phase clocking system for controlling the transfer of electrical charges through the transfer channels. Suitable circuitry for performing this function is well known in the art and may also be included in the form of integrated circuitry, if desired. Electrical output signals from the storage elements 51 are obtained from suitable output circuitry 54 which may, for example, include P-N junctions associated with each transfer channel or a single P-N junction which interconnects all output channels. Alternately, various combinations of P-N junctions or other suitable devices such as those described in our con-currently filed application No. 40962/71 (Serial No. 1,343,174) may be employed for extracting surface charges from the array of storage elements 51. The output signal derived from the output circuitry 54 is illustrated in FIGURE 4 as a video output signal, such as that obtained from a camera tube.

The operation of the embodiment illustrated in FIGURE 4 is easily understood by considering the timing relationship of signals applied to the image converter 50 during a cycle of operation. For example, if a cycle of operation is divided between read-in and read-out, then during the read-in time, depletion region forming voltages are applied to all hold lines. During this time electromagnetic radiation incident on the semiconductor generates minority carriers which are stored and integrated in the potential wells. During the read-out time, the stored electric charges are sequentially read-out on a row-by-row basis by applying transfer signals, such as ϕ_1 and ϕ_3, for example, to the transfer lines and sequentially removing the depletion region forming voltages from the hold lines so that the electrical charges from each row are sequentially read-out to the output circuitry 54. The release of selected electrical charges on a row-by-row basis is desirably synchronized with the application of a transfer signal applied to a transfer line overlying the cellule and the opening interconnecting the cellule and the channel. More specifically and with reference to FIGURE 1 of the drawing, read-out of electrical charges from row one is desirable initiated by the removal of the depletion region forming voltage V_1 from hold line 22 at the same time that voltages (i.e., ϕ_2) are being applied to charge transfer lines 25, 27 and 29. In this way, the stored electrical charges are always under the influence of an electric field and are hence not permitted to return to the bulk semiconductor. Read-out from each of the other rows is also synchronized in the same manner. This method of operation substantially reduces the loss of any portion of the electrical charges to the bulk semiconductor and hence enhances the transfer of electrical charges along the surface of the semiconductor substrate. In addition to being useful as an image converter, the storage and transfer apparatus of the instant invention can also be employed for the storage and transfer of digital information. For example, digital information may be introduced into the storage and transfer apparatus by the P-N junction 40 while the depletion region forming voltage is removed from the conductor member 22. As the electrical charges are moved down the transfer channel, at some point in time the depletion region forming voltage is applied to conductor member 22 and the electrical charges in the transfer channel are quickly swept to the depletion region potential wells underlying the cellules since these depletion regions are much deeper than those in the channel 21. Once stored in the potential wells, the electrical charges may be held for a suitable period of time and then transferred to another location or to output circuitry for performing logic functions, if desired. Those skilled in the art can readily appreciate that one of the most desirable characteristics of our invention is the ability to hold electric charges representative of information for selectively variable periods of time and to release selected electric charges merely by removal of a depletion region forming voltage from a conductor member hold line. Conversely, charges may be stored in the surface-adjacent portions of the semiconductor substrate merely by applying a depletion region forming voltage.

WHAT WE CLAIM IS:—

1. A conductor-insulator-semiconductor device comprising: a substrate of semiconductor material, an insulator layer which overlies a major surface of said substrate and which

device which does not require the use of a scanning electron beam has great commercial utility.

A particularly useful embodiment of our invention is illustrated in FIGURE 4 wherein a two-dimensional optical image converter 50 comprising an integrated array of CIS storage elements 51 are arranged in an "X-Y Pattern" on a semiconductor substrate. The storage elements and the transfer channels are substantially similar to those described above and operate in substantially the same manner. The optical image converter 50 further comprises row select generator circuitry 52 which may, for example, be fabricated on the semiconductor substrate as integrated circuitry and include the necessary circuitry to scan each row and provide the depletion region forming voltages to the appropriate conductor member hold lines during the read-in times and to selectively remove these voltages during the read-out times. The optical image converter 50 also includes a transfer control generator 53, which may, for example, includes a two- or three-phase clocking system for controlling the transfer of electrical charges through the transfer channels. Suitable circuitry for performing this function is well known in the art and may also be included in the form of integrated circuitry, if desired. Electrical output signals from the storage elements 51 are obtained from suitable output circuitry 54 which may, for example, include P-N junctions associated with each transfer channel or a single P-N junction which interconnects all output channels. Alternately, various combinations of P-N junctions or other suitable devices such as those described in our con-currently filed application No. 40962/71 (Serial No. 1,343,174) may be employed for extracting surface charges from the array of storage elements 51. The output signal derived from the output circuitry 54 is illustrated in FIGURE 4 as a video output signal, such as that obtained from a camera tube.

The operation of the embodiment illustrated in FIGURE 4 is easily understood by considering the timing relationship of signals applied to the image converter 50 during a cycle of operation. For example, if a cycle of operation is divided between read-in and read-out, then during the read-in time, depletion region forming voltages are applied to all hold lines. During this time electromagnetic radiation incident on the semiconductor generates minority carriers which are stored and integrated in the potential wells. During the read-out time, the stored electric charges are sequentially read-out on a row-by-row basis by applying transfer signals, such as ϕ_1 and ϕ_2, for example, to the transfer lines and sequentially removing the depletion region forming voltages from the hold lines so that the electrical charges from each row are sequentially read-out to the output circuitry 54. The release of selected electrical charges on a row-by-row basis is desirably synchronized with the application of a transfer signal applied to a transfer line overlying the cellule and the opening interconnecting the cellule and the channel. More specifically and with reference to FIGURE 1 of the drawing, read-out of electrical charges from row one is desirable initiated by the removal of the depletion region forming voltage V_1 from hold line 22 at the same time that voltages (i.e., ϕ_2) are being applied to charge transfer lines 25, 27 and 29. In this way, the stored electrical charges are always under the influence of an electric field and are hence not permitted to return to the bulk semiconductor. Read-out from each of the other rows is also synchronized in the same manner. This method of operation substantially reduces the loss of any portion of the electrical charges to the bulk semiconductor and hence enhances the transfer of electrical charges along the surface of the semiconductor substrate. In addition to being useful as an image converter, the storage and transfer apparatus of the instant invention can also be employed for the storage and transfer of digital information. For example, digital information may be introduced into the storage and transfer apparatus by the P-N junction 40 while the depletion region forming voltage is removed from the conductor member 22. As the electrical charges are moved down the transfer channel, at some point in time the depletion region forming voltage is applied to conductor member 22 and the electrical charges in the transfer channel are quickly swept to the depletion region potential wells underlying the cellules since these depletion regions are much deeper than those in the channel 21. Once stored in the potential wells, the electrical charges may be held for a suitable period of time and then transferred to another location or to output circuitry for performing logic functions, if desired. Those skilled in the art can readily appreciate that one of the most desirable characteristics of our invention is the ability to hold electric charges representative of information for selectively variable periods of time and to release selected electric charges merely by removal of a depletion region forming voltage from a conductor member hold line. Conversely, charges may be stored in the surface-adjacent portions of the semiconductor substrate merely by applying a depletion region forming voltage.

WHAT WE CLAIM IS:—

1. A conductor-insulator-semiconductor device comprising: a substrate of semiconductor material, an insulator layer which overlies a major surface of said substrate and which

* C L M S *

is formed to present a plurality of cellules communicating with a common channel, a conductor member overlying said cellules, means for causing storage of electrical charges in the surface-adjacent portions of said substrate substantially underlying said cellulose, and means for transferring selected electrical charges between the surface-adjacent portions of said substrate underlying said cellules and said channel.

2. A device as claimed in Claim 1 wherein such electrical charges are formed by the movement of minority carriers to the surface-adjacent portions of the substrate underlying said cellules, said minority carriers being generated in response to electromagnetic radiation incident on said substrate.

3. A device as claimed in Claim 1 or Claim 2 wherein said means for causing storage includes means for applying a voltage to said conductor member to cause formation of potential wells in the surface-adjacent portions of said substrate substantially underlying said cellules.

4. A device as claimed in any one of Claims 1 to 3 wherein said means for transferring includes a plurality of transfer lines overlying said common channel and wherein the transfer of electrical charges is effected by sequentially applying depletion region forming voltage to adjacent transfer lines to incrementally move the electrical charges along the surface-adjacent portions of said substrate underlying said channel.

5. A device as claimed in Claim 4 wherein said transfer lines comprise a plurality of conductors insulating overlying said common channel.

6. A device as claimed in Claim 5 wherein said transfer lines are spaced apart and are in overlapping relation with each other in plan view.

7. A device as claimed in any one of Claims 4 to 6 wherein at least some of said transfer lines each overlie a cellule, a common channel and the communications therebetween.

8. A device as claimed in any one of Claims 1 to 7 wherein said cellules are arranged in rows with a common channel associated with each row and a conductor member overlying each row of cellules, and including means operable to permit release of stored electrical charges from a selected row of cellules to its row-associated channel while holding electrical charges in other rows.

9. A device as claimed in Claim 8 including means for receiving the electrical charges released to said row-associated channel.

10. A device as claimed in Claim 8 wherein said means for transferring includes column-associated means for moving the released electrical charges along the row-associated channel.

11. A device as claimed in Claim 1 including a P-N junction associated with said common channel, whereby such charges may be introduced to said substrate.

12. A device as claimed in any one of Claims 1 to 10 wherein said electrical charges are introduced into and removed from a row-associated channel with a send-receive device.

13. A device as claimed in any one of the preceding Claims wherein the non-selected electrical charges stored in the surface-adjacent portions of said substrate are stored at a sufficiently low potential to be substantially unaffected by the means for transferring the selected charges.

14. A conductor-insulator-semiconductor device substantially as described herein with reference to Figures 1 to 3 of the accompanying drawings.

15. An electro-opertical converter including a device as claimed in any one of the preceding Claims.

16. An electro-optical converter substantially as described herein with reference to the accompanying drawings.

BROOKES & MARTIN,
High Holborn House,
52/54, High Holborn,
London, W.C.1.,
Agents for the Applicants.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1974.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

