

PSEUDO PRECISE I-CACHE INCLUSIVITY FOR VERTICAL CACHES**ABSTRACT**

A modified MESI cache coherency protocol is implemented within a level two (L2) cache (114, 116) accessible to a processor having bifurcated level one (L1) data and instruction cache (106,108,110,112). The modified MESI protocol includes two substates (310,312) of the shared state (306), which denote the same coherency information as the shared state (306) plus additional information regarding the contents/coherency of the subject cache entry. Upon entering the first substate (310), the coherency state (310) does not transition to the invalid state (308) unless an operation designed to invalidate instructions is received. Local processor operations contravening the presumption that the contents comprise instructions may cause the coherency state (310) to transition to an ordinary shared state (306). Since the contents of a cache entry in both coherency substates (310,312) are presumed to be instructions, not data, instructions within an L2 cache (114,116) are not discarded as a result of snooped flushes, but are retained for possible reloads by a local processor (247).

Fig.1