

STACKED DIE PACKAGES

ABSTRACT

A stacked die semiconductor package that includes a substrate with a plurality of adhesive portions arranged in a manner to create at least one gap between the adhesive portions. The package also includes a first semiconductor chip having a non-active surface in contact with the adhesive portions, and an active surface being electrically connected to the substrate. In the package, a second semiconductor chip the non-active surface of the second semiconductor chip is attached to the non-active surface of the first semiconductor chip by a layer of adhesive therebetween. The active surface of the second semiconductor chip is electrically connected to the substrate. An encapsulant material covers the first and second semiconductor chips and their associated electrical connections. The encapsulating material fills the at least one gap between the plurality of adhesive portions and thereby encapsulates the second semiconductor chip and its associated electrical connection.

Figure 4A