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(54) Title: METHOD AND APPARATUS FOR FAST DECODING OF OOH AND OFH MAPPED INSTRUCTIONS

(57) Abstract

A method and apparatus for fast decoding of OOH and OFH mapped instructions. A set of instruction bytes are selected for length decoding. Instruction bytes that contain no length information, such as OFH opcode bytes in the Intel architecture instruction set, are detected and shifted out of the set before length decoding to determine the length of an instruction is performed on the set. Removing instruction bytes that contribute no length information allows the length decoder logic (40) to be optimized for size and speed. In one embodiment, parallel length decoder sets (35) that each include a detector (36), shifter (38), and length decoder (40) operate in parallel on a line of instruction bytes prefetched from an instruction cache (30). In one embodiment, the length decoders are PLAs (programmable logic arrays 37) that are combined with separate shifters and detectors logic (12-15). This embodiment advantageously allows smaller PLA length decoders (37). In another embodiment, each set of detector, shifter, and length decoder is implemented in a single PLA (37). In this embodiment, the detector/shifter/length decoder PLAs (37) are larger but can be optimized for greater overall speed. The present invention is advantageously used to determine the length of multiple variable length instructions before the instructions are decoded for execution.

