

PLL CIRCUIT, PHASE SHIFTING METHOD, AND IC CHIP

ABSTRACT OF THE DISCLOSURE

A PLL circuit includes: a clock signal generating unit for generating a first clock signal and a second clock signal of which the phase differs from the first clock signal by $\pi/2$; a computing unit for computing first phase comparison results showing the results of comparing the phases of a signal wherein the first clock signal is subjected to phase shifting with the PSK modulation signal, and second phase comparison results showing the results of comparing the phases of a signal wherein the second clock signal is subjected to phase shifting with the PSK modulation signal, based on first and second parameters, the first clock signal, the second clock signal, and the PSK modulation signal; a control direction setting unit for virtually controlling the control angle; a parameter control unit; and a reading control unit for controlling the timing of reading data from the PSK modulation.

Figure 1