Abstract of the Disclosure

METHODS OF FORMING ELECTRICAL INTERCONNECT STRUCTURES USING POLYMER RESIDUES TO INCREASE ETCHING SELECTIVITY THROUGH DIELECTRIC LAYERS

A method of fabricating interconnections of a microelectronic device includes providing a semiconductor substrate comprising a lower dielectric layer and a lower interconnection. An etch stopper layer and an interlayer dielectric layer is formed on the semiconductor substrate followed by a via hole in the interlayer dielectric layer so that the etch stopper layer is exposed through the via hole. The etch stopper layer is carbon doped and a trench is formed in the interlayer dielectric layer so that the trench overlaps part of the via hole. The carbon-doped etch stopper layer is removed and the via hole and the trench is filled with a conductive material to form an upper interconnection.

Fig. 2E