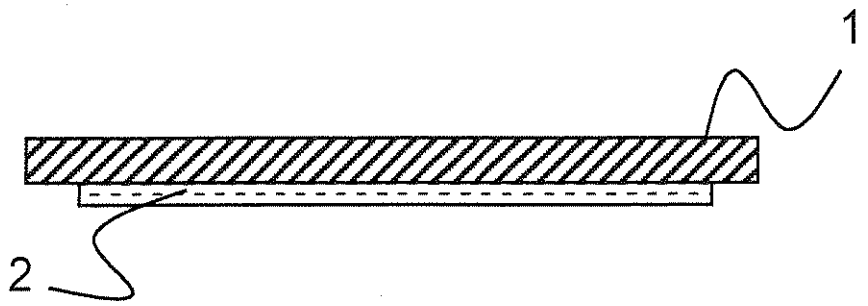


Fig. 1

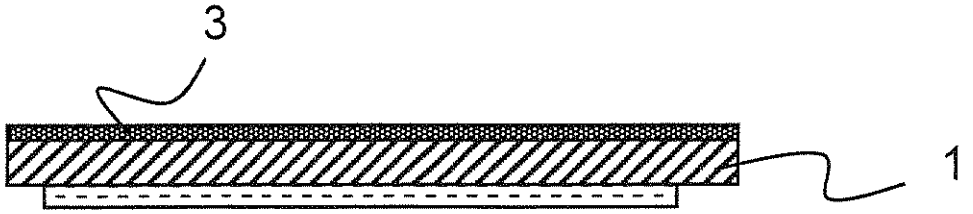


Fig. 2

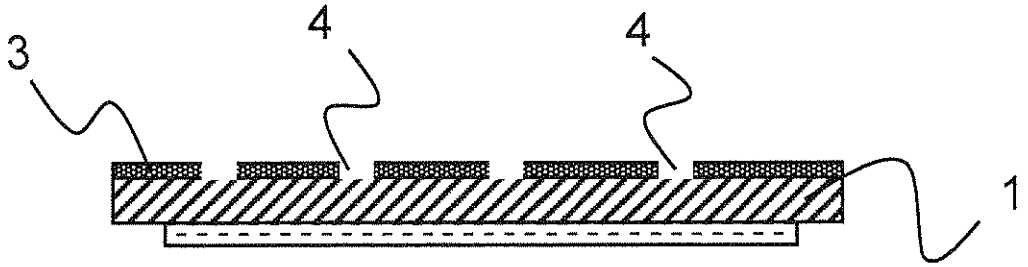


Fig. 3

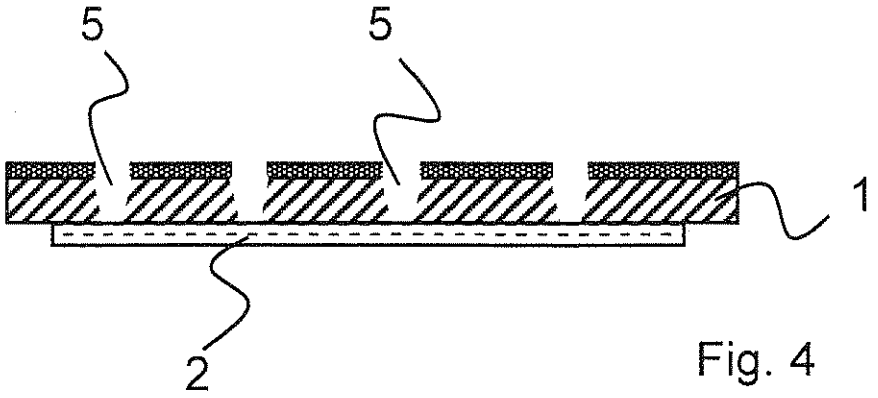


Fig. 4

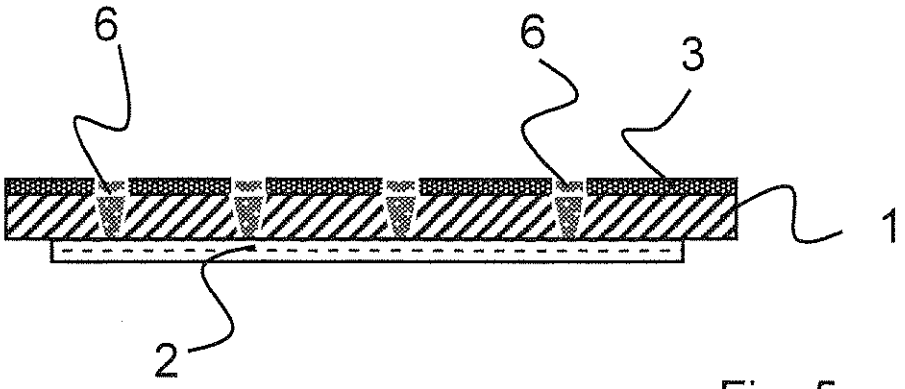


Fig. 5

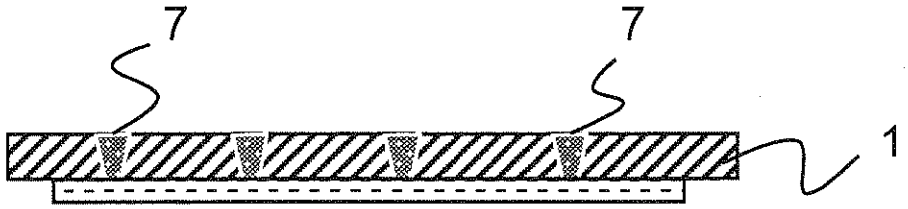


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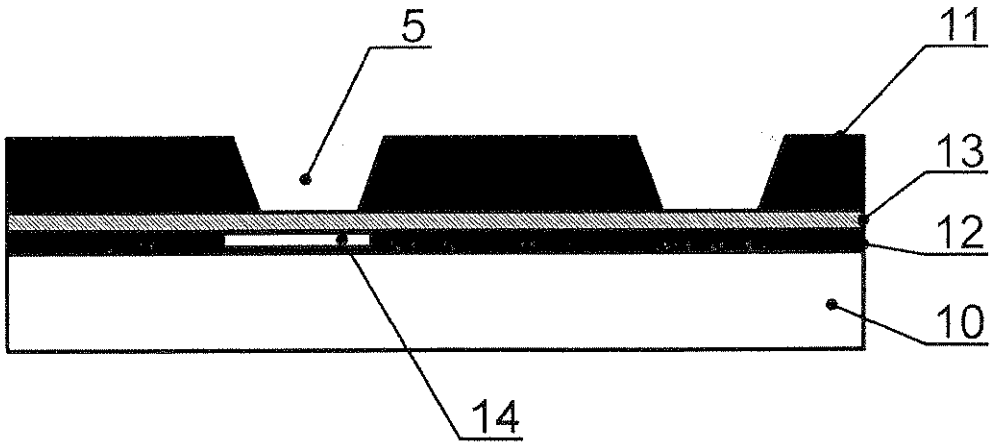


Fig. 7

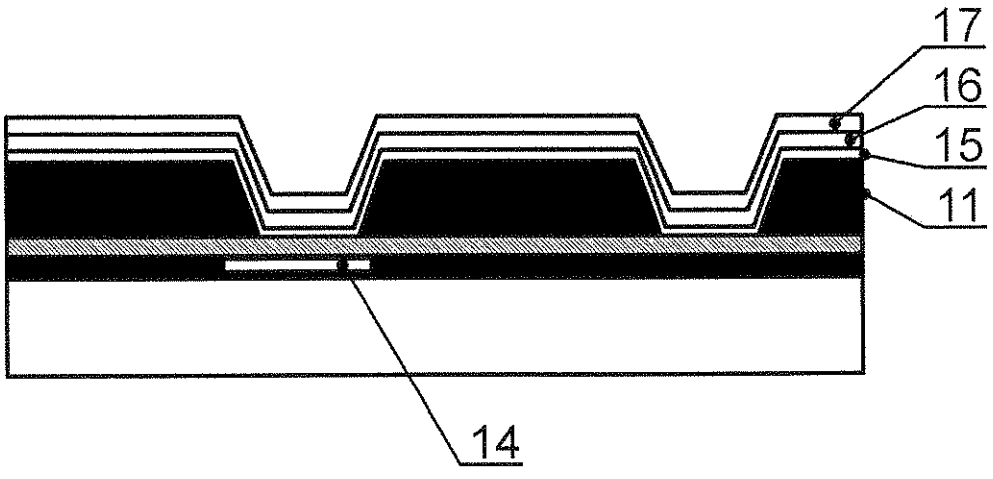


Fig. 8

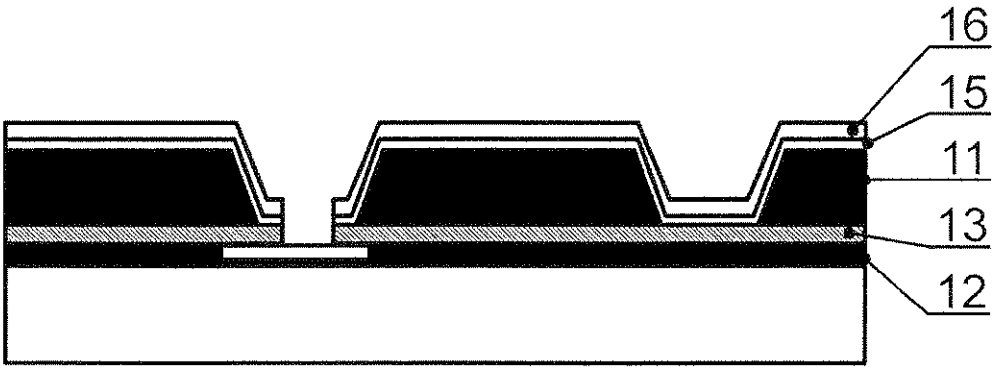


Fig. 9

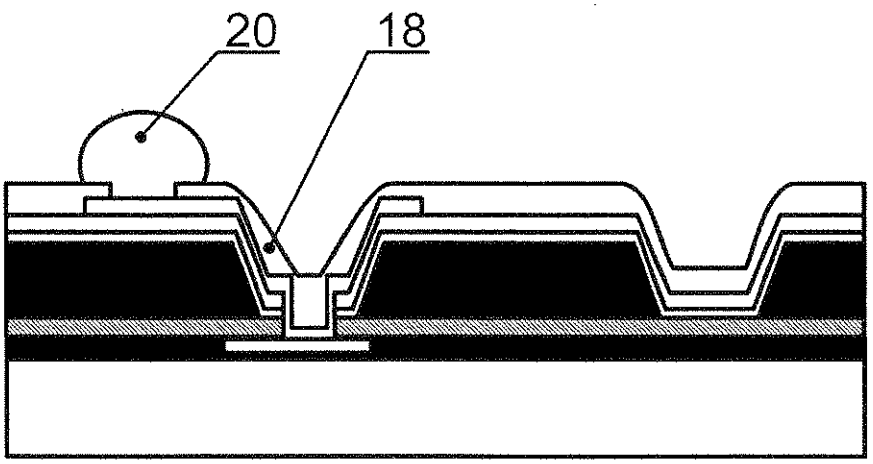


Fig. 10

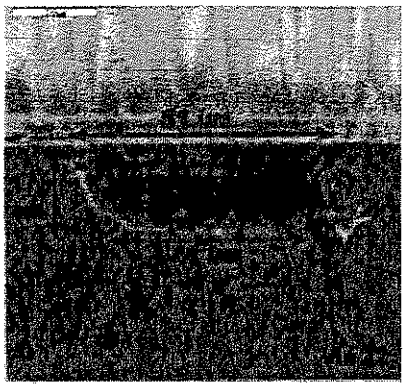


Fig. 11

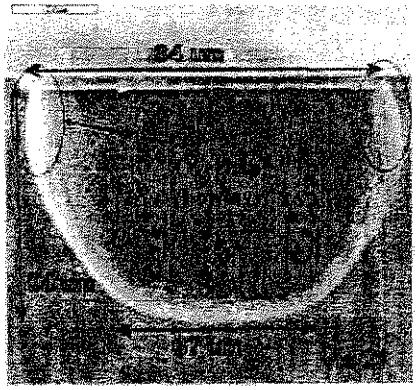


Fig. 12

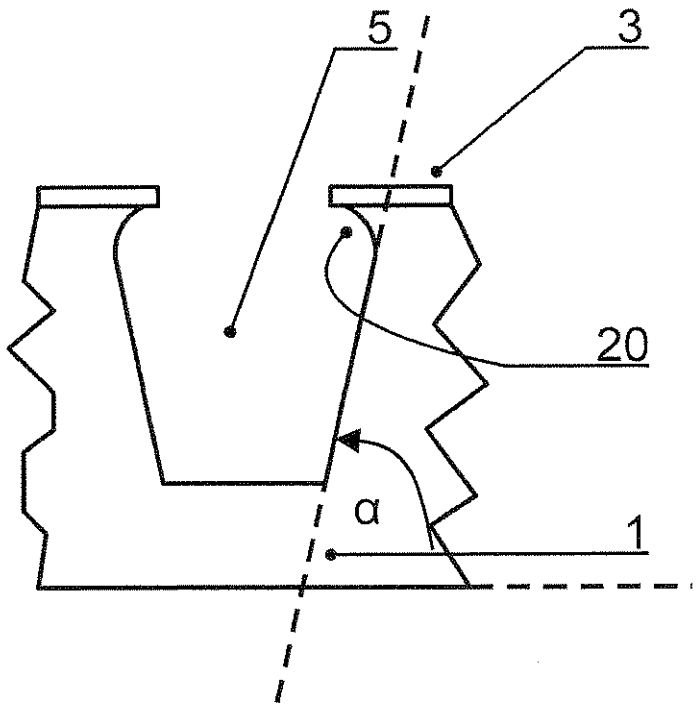


Fig. 13

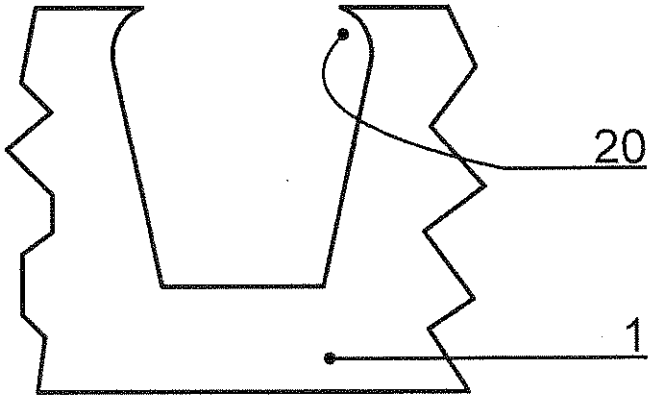


Fig. 14

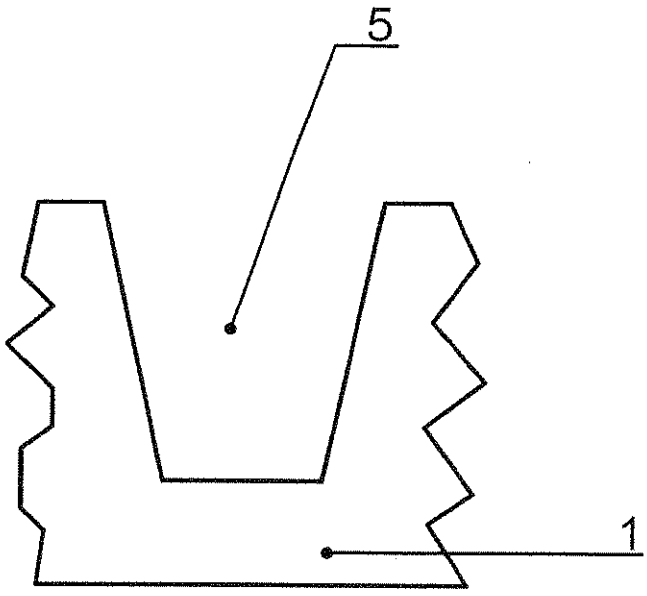


Fig. 15

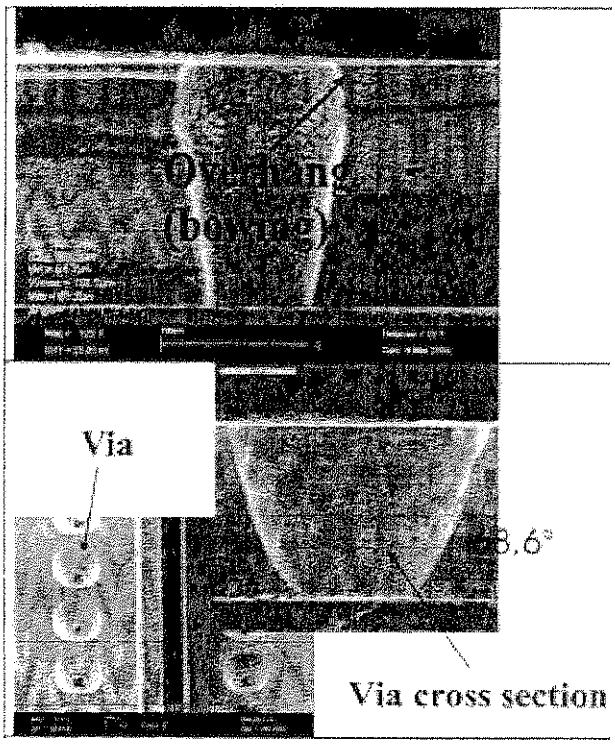


Fig. 16

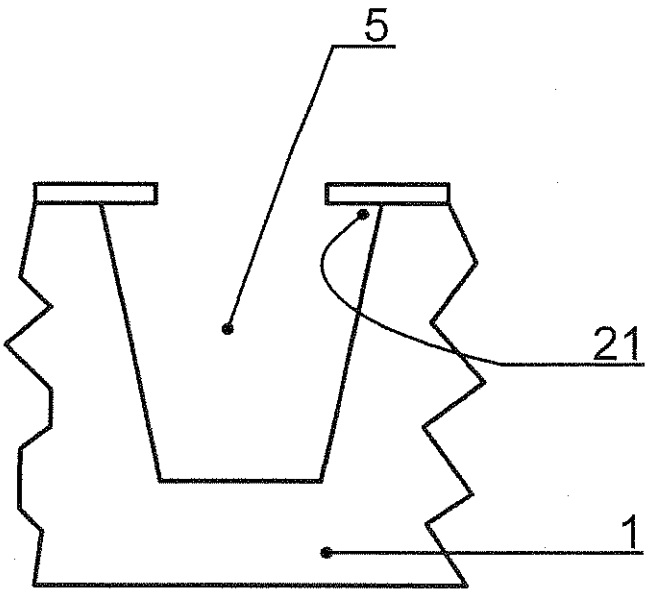


Fig. 17

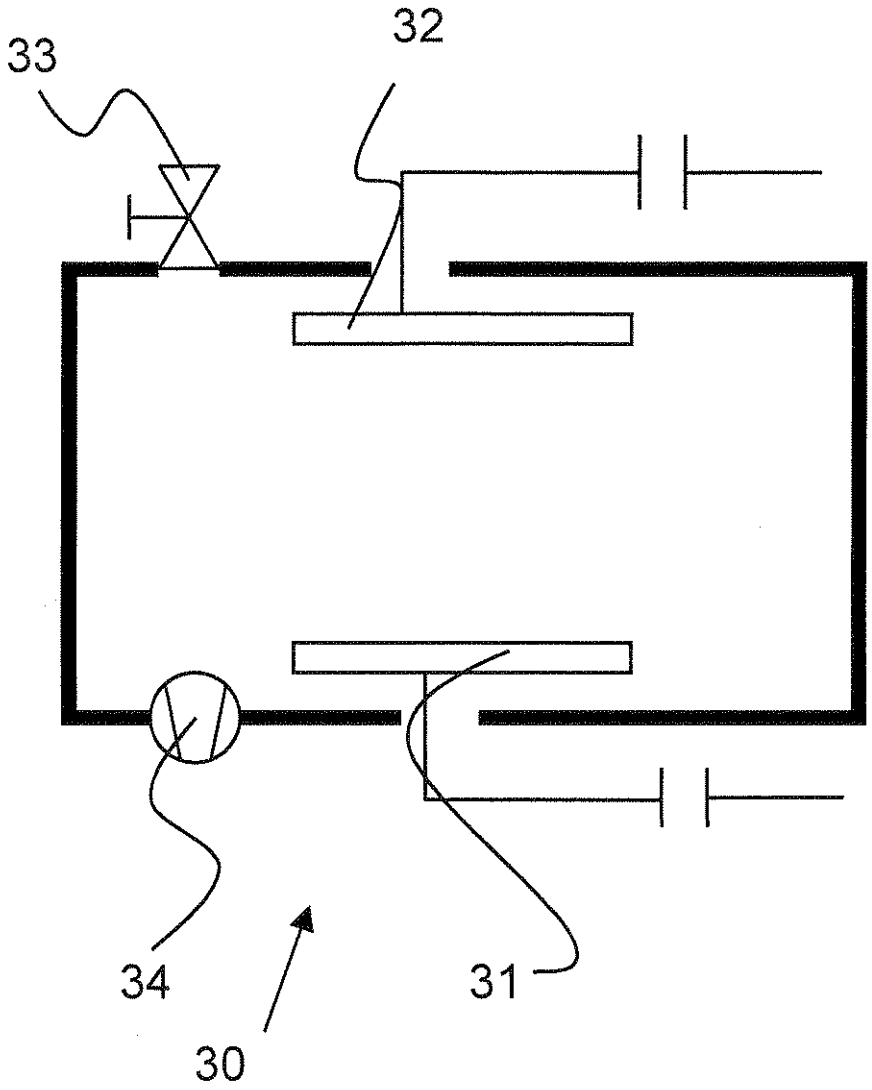


Fig. 18

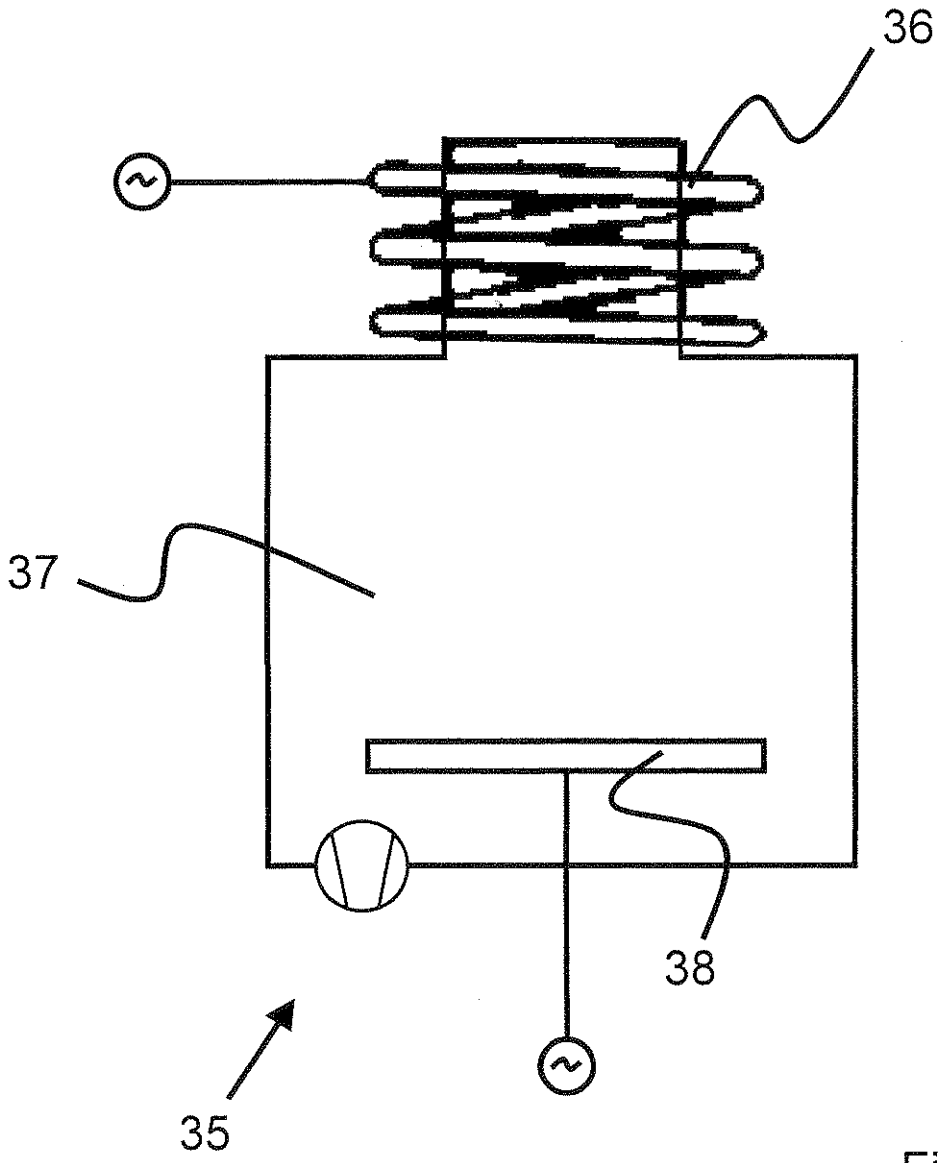


Fig. 18a

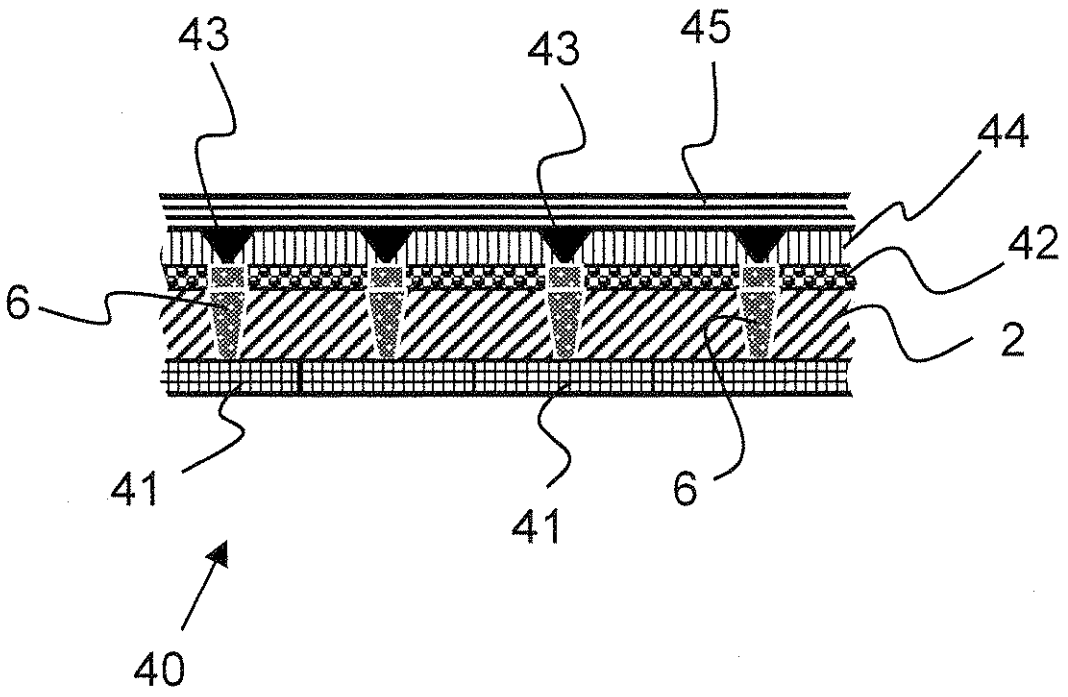


Fig. 19

Wafer Level Chip Size Packaging

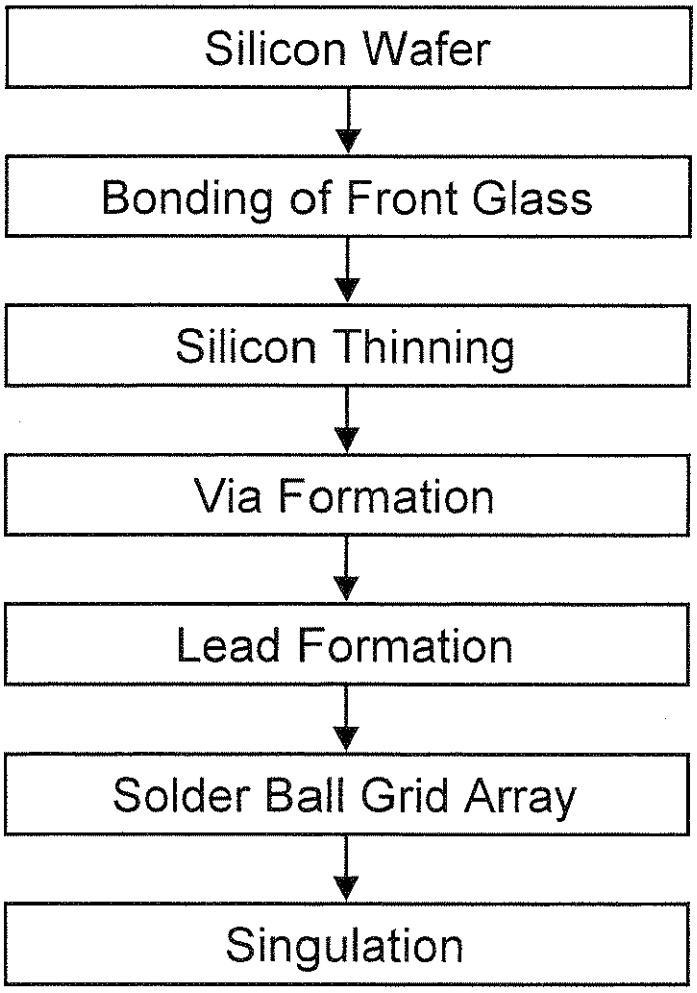


Fig. 20

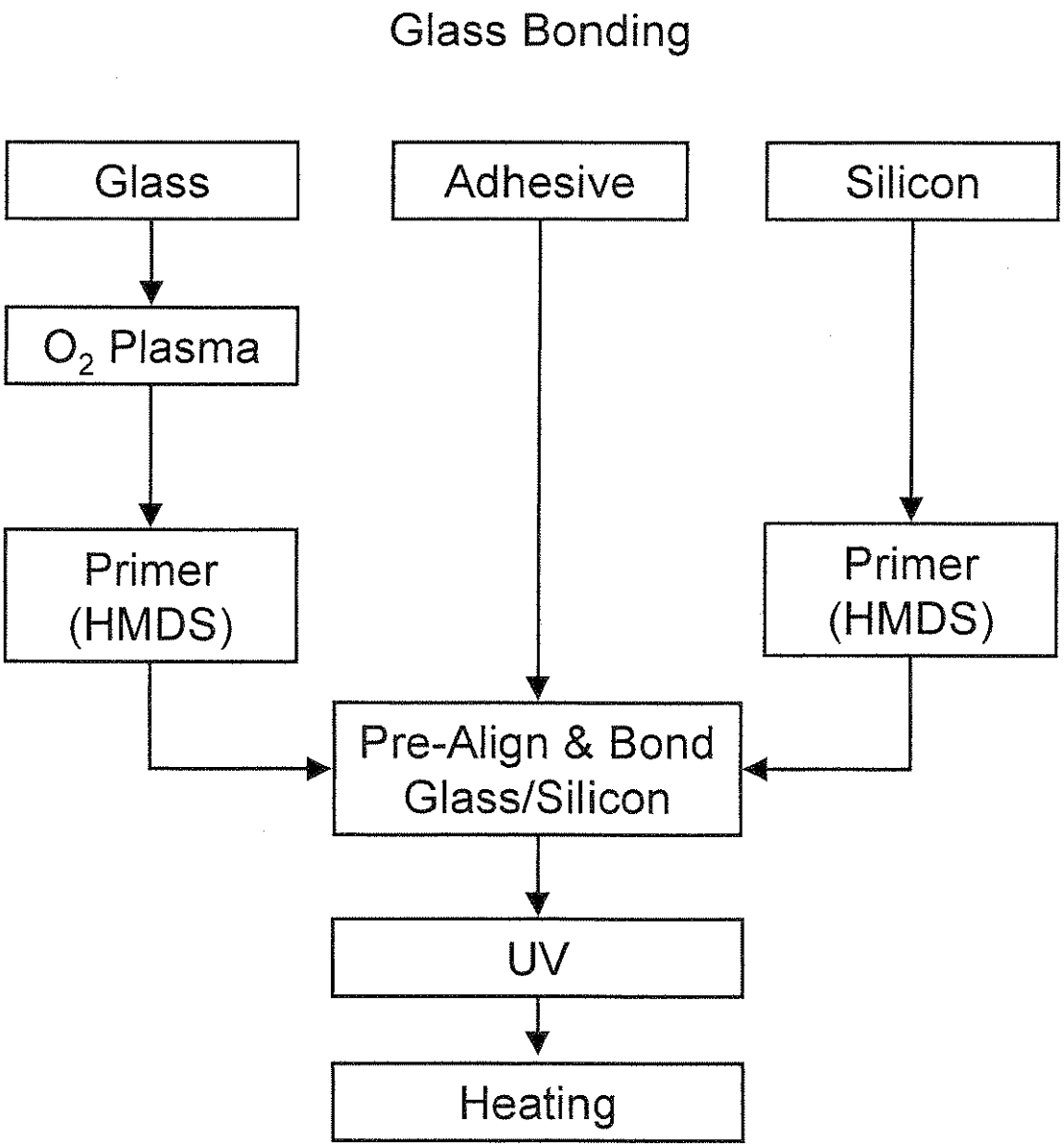

Glass Bonding
Glass
Adhesive
Silicon
O_2 Plasma
Primer (HMDS)
Primer (HMDS)
Pre-Align & Bond Glass/Silicon
UV
Heating

Fig. 21

Silicon Thinning

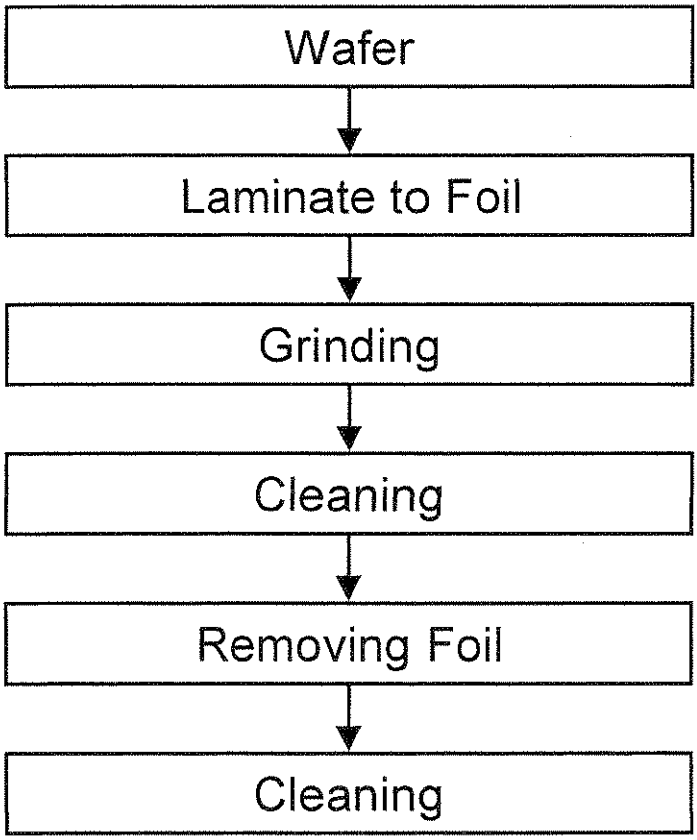


Fig. 22

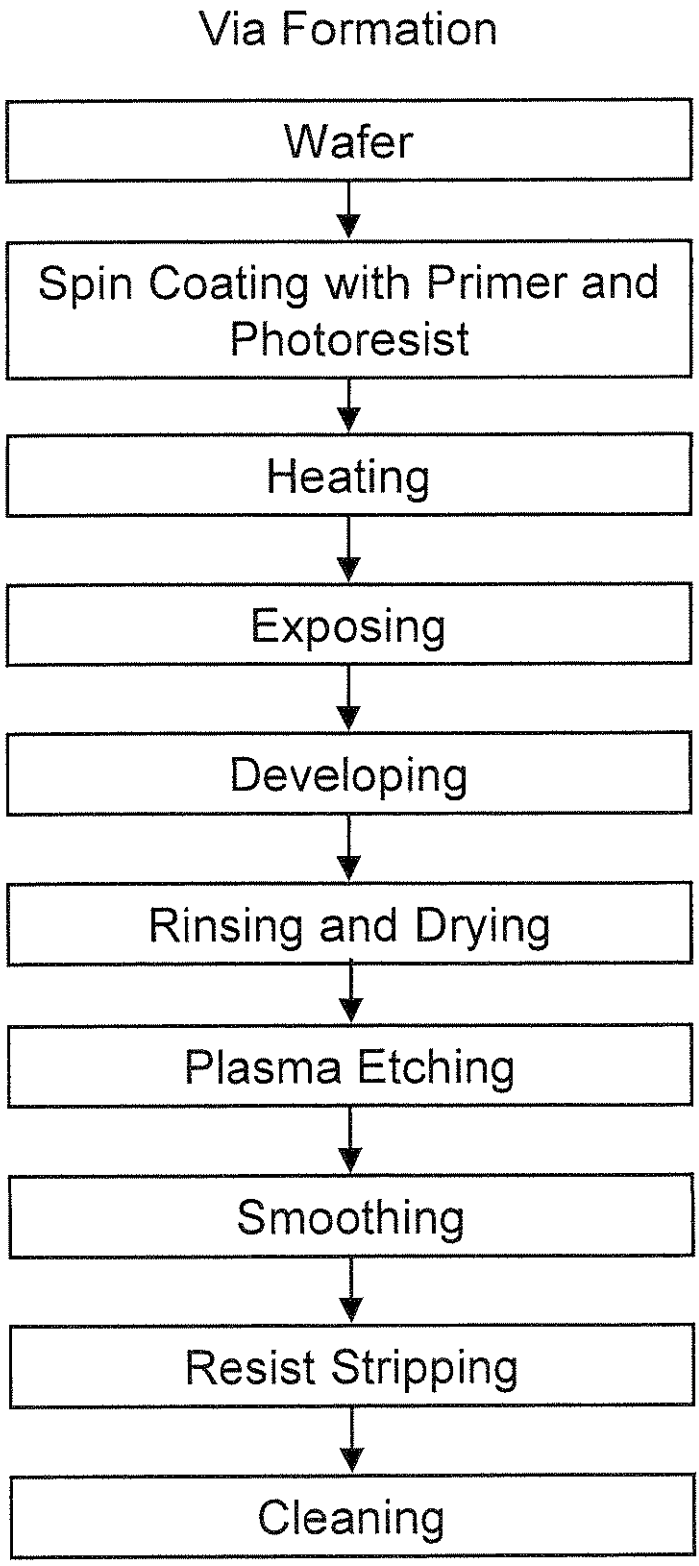

Via Formation
Wafer
Spin Coating with Primer and Photoresist
Heating
Exposing
Developing
Rinsing and Drying
Plasma Etching
Smoothing
Resist Stripping
Cleaning

Fig. 23

Insulator Deposition

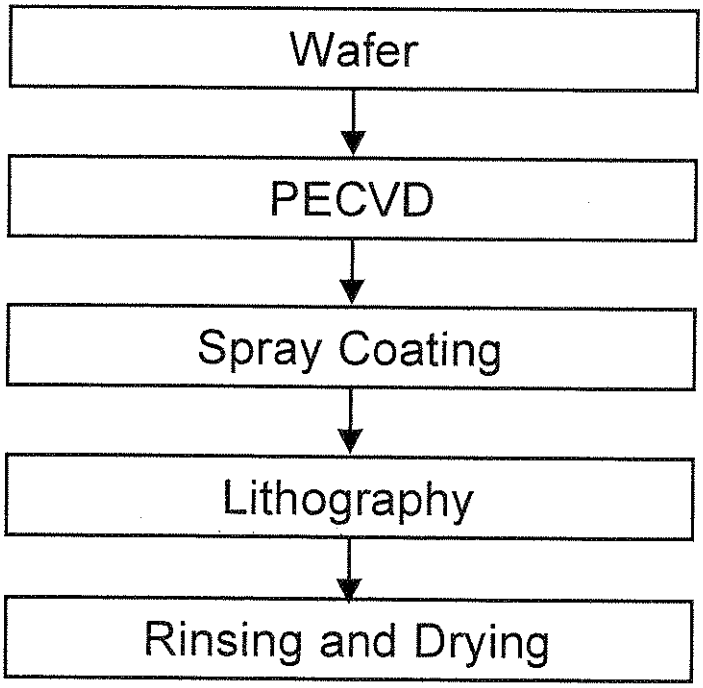


Fig. 24

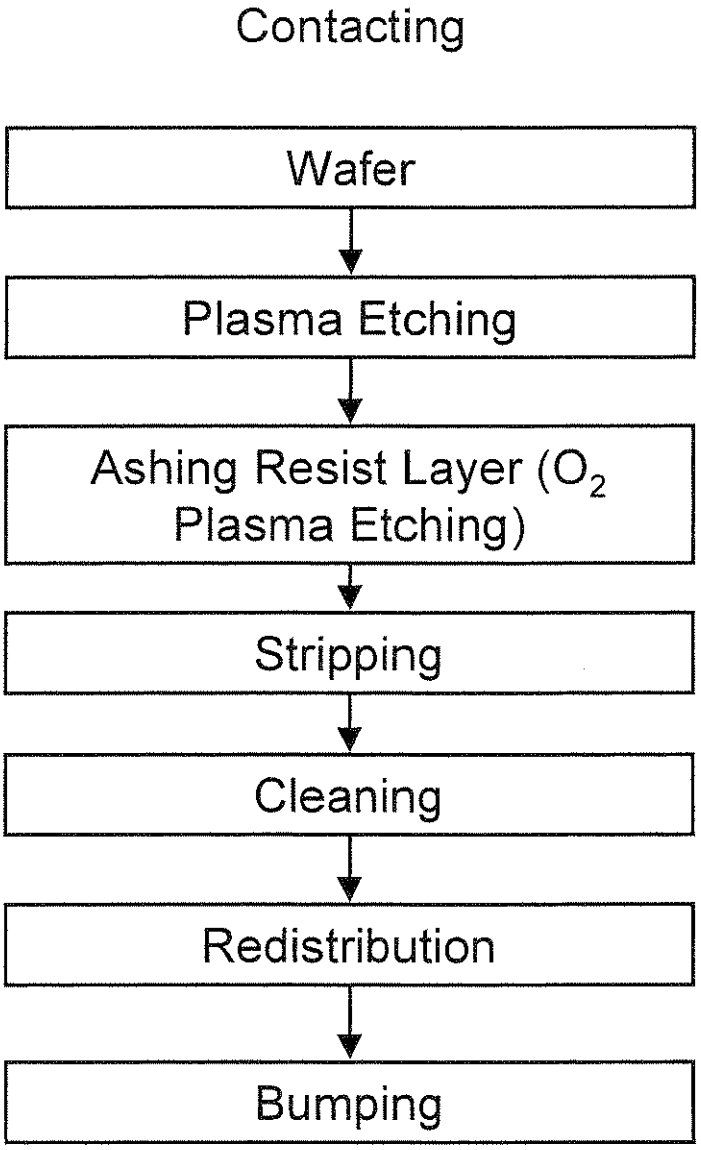

Contacting
Wafer
Plasma Etching
Ashing Resist Layer (O_2 Plasma Etching)
Stripping
Cleaning
Redistribution
Bumping

Fig. 25