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BASIC CELL ARCHITECTURE FOR MASK PROGRAMMABLE GATE ARRAY

Abbas El Gamal

CROSS-REFERENCE TO RELATED APPLICATION

This application is related to copending Application Serial No. 07/524,183, issued as Patent No. 5,055,716, entitled "Basic Cell for BiCMOS Gate Array," by Abbas El Gamal, incorporated herein by reference.

FIELD OF THE INVENTION

This invention relates to integrated circuits and in particular to Application Specific Integrated Circuits, which include programmable gate arrays.

BACKGROUND OF THE INVENTION

Programmable gate arrays, sometimes containing over one million transistors, are frequently used to create economical Application Specific Integrated Circuits (ASIC). A programmable gate array may be metal mask programmable, electrically programmable, or laser programmable. In a mask programmable gate array, the silicon die containing the unconnected transistors is called a master slice or master image. A user who wishes to customize a master slice uses well-known software programs and predefined logic circuit configurations (macrocells) contained in a macrocell library to selectively interconnect the transistors within the gate array to provide an ASIC.

In one type of metal mask programmable gate array, an array of cells is formed on a chip wherein each cell is comprised of a plurality of unconnected components. In a typical arrangement, there is a variety of types of components in each cell to enable a designer of the macrocells to create various kinds of logic circuits within each cell or by using a combination of cells.

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Ideally, each cell should contain an optimum number and variety of components so that the designer may create a wide variety of macrocells using the shortest interconnect wire lengths, using a minimum amount of die area, and using other techniques for achieving high performance for each macrocell.

In a programmable gate array structure, CMOS transistors frequently comprise the components of a cell due to the low power consumption of a CMOS device, where an N-channel and a P-channel MOSFET are connected in series between a power supply terminal and ground. Because the gates of these CMOS transistors are made common, one transistor will be off while the other transistor will be on, thus avoiding a low impedance path between the power supply terminal and ground. These CMOS transistors may be used as building blocks to create a wide variety of macrocells.

A conventional CMOS gate array cell is shown in Fig. 1 and comprises a number of equal size N-channel transistors 2 and a number of equal size P-channel transistors 4. Such a cell is inefficient at implementing memory elements such as D-type flip flops and SRAM cells, and its output drive capability is very limited. The transistor sizes typically used in such prior art cells are unnecessarily large for driving nets with a low fanout of, for example, one or two and are insufficient for driving nets with a high fanout exceeding, for example, five. Consequences of using unnecessarily large transistor sizes for driving low fanouts are that the relatively large input capacitances for the logic macrocells result in unnecessarily high dynamic power dissipation and also unnecessarily high loading on clock nets.

Since the typical transistors are too small to adequately drive a fanout exceeding five, two or more macrocells must be connected in parallel, or separate buffers must be introduced in the design. These large

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resulting macrocells give rise to inefficient chip area utilization and an increase in interconnect length.

Also in the prior art, to improve the efficiency of implementing SRAM cells, CMOS gate array cells with N-channel transistors of two different sizes have been used. The smaller size N-channel transistors are typically less than one third the size of the larger size N-channel transistors. These prior art cells may also incorporate small size P-channel transistors to perform various functions. However, in such cells, the large transistors are still unnecessarily large for driving low fanout nets and inadequate for driving high fanout nets, while the small transistors are inadequate for driving almost all nets. Generally, for these prior art devices to drive high fanout nets, two or more macrocells must be connected in parallel or separate buffers must be introduced.

In the prior art, since the small size transistors used in SRAMs are typically not used for implementing logic macrocells, such as D-flip flops, these logic macrocells are area inefficient. Moreover, the input capacitance for the macrocells is generally unnecessarily high.

SUMMARY OF THE INVENTION

A highly efficient CMOS cell structure for use in a metal mask programmable gate array, such as a sea-of-gates type gate array, is disclosed herein. In a basic cell, in accordance with one embodiment of the invention, three or more sizes of N-channel transistors and three or more sizes of P-channel transistors are used. The larger size transistors are incorporated in a drive section of a cell, while the smaller size transistors are incorporated in a compute section of a cell. The larger size transistors may be used for driving high fanout nets and even used to perform logic functions, while the smaller transistors may

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be used to implement SRAM cells and logic functions and for driving low fanout nets.

The particular transistors in the compute and drive sections, and the arrangements of the transistors in the compute and drive sections, provide a highly efficient use of silicon real estate while enabling the formation of a wide variety of macrocells to be formed.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a basic prior art cell;

Fig. 2 shows a basic cell schematic for a preferred embodiment cell in a mask programmable sea-of-gates structure;

Figs. 3a and 3b illustrate an SRAM built using a single compute section of the cell of Fig. 2;

Figs. 4-7 show various logic circuits or macrocells which may be implemented with the cell structure and array layout shown in Figs. 2 and 8;

Figs. 8a and 8b illustrate sample tiling of the compute and drive sections in a mask programmable sea of gates structure;

Fig. 9 shows a preferred layout for a single compute section in the basic cell structure of Fig. 2;

Figs. 10a-10c illustrate drive sections which may be used in conjunction with the compute sections of this invention;

Fig. 11 illustrates a basic cell in accordance with the invention;

Fig. 12 illustrates an ASIC device incorporating a gate array.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the invention is illustrated in Fig. 2, where a single mask programmable gate array cell contains one or more compute sections 6, 8, 10 and may contain a drive sections 12 or share a drive section with another cell. The mask programmable gate

array cell shown in Fig. 2 comprises N-channel transistors of three different sizes and P-channel transistors of three different sizes. The largest N-channel transistors 14, 15 and the largest P-channel transistors 16, 17 are located in drive section 12 and have channel widths larger than any transistors in compute sections 6, 8, 10. The medium size P-channel transistors 18-23 and medium size N-channel transistors 24-29 are approximately half the size of the large P and N-channel transistors 14-17. The small N-channel transistors 30-35 are between approximately one-half and one-third the size of the P and N-channel medium size transistors 18-29, and the small P-channel transistors 36-41 are smaller than the small N-channel transistors 30-35. The particular channel widths and lengths (W/L) used in the preferred embodiment are illustrated in Fig. 2. Each compute section 6, 8, 10 is preferably identical.

The preferred embodiment of the cell shown in Fig. 2 comprises three compute sections 6, 8, 10 and one drive section 12, but any number of compute sections and drive sections may be placed adjacent to one another to form a single cell. A single compute section 6, 8, or 10 comprises two medium size N-channel transistors (e.g., 24, 25), two small N-channel transistors (e.g., 30, 31), two medium size P-channel transistors (e.g. 18, 19), and two small P-channel transistors (e.g., 36, 37).

The small and medium size transistors in two compute sections may be used to implement two, six-transistor SRAM cells, one of which is shown in Fig. 3a. In Fig. 3a, the small P-channel transistors 36, 37 are used as pull-up transistors in CMOS inverters 50 and 52, while the medium N-channel transistors 24, 25 are used as pull-down transistors in inverters 50 and 52. This is illustrated in Fig. 3b, which shows CMOS inverter 50 or 52. Small N-channel transistors 30, 31 are used as pass transistors in the SRAM of Fig. 3a.

The D-flip flop of Fig. 4 may be constructed using the complete cell of Fig. 2, having three compute sections. Each of the inverters is formed using a medium P-channel transistor (or a medium in parallel with a small P-channel transistor) and a medium N-channel transistor. Other transistors used in Fig. 4 are shown with their relative sizes.

Macrocells for driving low fanout nets (e.g., one to two nets) may be implemented using only medium and small size transistors, such as the NAND gate of Fig. 5, using only a single compute section. In Fig. 5, serially connected N-channel transistors 60, 62 are medium size. Small and medium size P-channel transistors 64, 66 are connected in parallel for additional drive capability.

Macrocells for driving medium fanout nets (e.g., three to five) may additionally use the large N and P-channel transistors residing in the drive section as logic devices, such as large N and P-channel transistors 70 and 72, respectively, illustrated in the four-input AND gate of Fig. 6.

For driving large fanout nets (e.g., greater than five nets), the transistors in two or more drive sections may be paralleled as shown in Fig. 7 where transistors 74-77 are large transistors.

As seen, the particular devices contained in each of the compute sections of a cell make highly efficient use of silicon real estate. In addition to the significant area savings achieved using the small and medium size transistors to implement logic macrocells, the use of such transistors reduces the input capacitive loading of the macrocells as compared to a conventional gate array. This is especially beneficial for reducing dynamic power dissipation and loading on clock nets.

The polysilicon and diffusion connections between the devices in each compute section of a cell are chosen to ensure routability between transistors within one or more cells to form macrocells. This is important since the

transistor sizes in the compute sections are significantly smaller than in a conventional gate array cell, which makes interconnections between the transistors in a cell more difficult.

The choice of the number of compute sections for a cell to the number of drive sections for the cell should be selected to optimize the density of useable gates (i.e., the number of gates per unit area). A low ratio of compute-to-drive sections has the advantage of high drive, but wastes area when implementing large macrocells such as D-flip flops and macrocells with low drive requirements such as SRAM cells. On the other hand, a high ratio of compute-to-drive sections, although more efficient for implementing low drive macrocells and D-flip flops, will result in inefficient implementation of small macrocells (e.g., those having two input gates) and high drive macrocells. The optimal ratio of compute sections-to-drive sections for a cell depends on the statistics of macrocell usage in the target designs and on the method of logic mapping.

Using an experimental approach, I have determined that a ratio of three compute sections for each drive section, as shown in Fig. 2, appears to achieve the best area utilization. The optimal ratio would, however, change if the macrocell usage statistics of the target designs change. In fact, it may be beneficial to use more than one ratio in the same master image. This is illustrated in Figs. 8a and 8b, where Fig. 8a shows a uniform master image with three compute sections (e.g., 80, 81, 82) being associated with one drive section (e.g., 83), and Fig. 8b shows a non-uniform master image with either four compute sections (e.g., 84-87) or two compute sections (e.g., 88, 89) associated with a single drive section (e.g., 90 or 91, respectively).

A preferred layout for each of the compute sections shown in Fig. 2 is shown in Fig. 9. In Fig. 9, the transistors are labelled to coincide with the transistors

in compute section 6 in Fig. 2. As seen from Fig. 9, a single polysilicon gate 100 is used for controlling transistors 18, 36, and 24 and a single polysilicon gate 102 is used for controlling transistors 19, 37, and 25. Separate gates 104 and 106 control N-channel transistors 30 and 31 so that these transistors may be operated independently, such as the pass transistors 30 and 31 used in the SRAM of Fig. 3. The N and P type source/drain diffusions for the various transistors are shown as the shaded areas in Fig. 9. As seen, the center diffusion for the medium and small P-channel transistors are made common by diffused P-type connector portion 110.

The structure of Fig. 9 may be formed using well known and conventional techniques.

By replacing the large P-channel transistors in drive section 12 of Fig. 2 with an NPN bipolar transistor, a BiNMOS-type driver may be added to the output of macrocells which results in significant performance improvement.

Other drive sections such as one containing two NPN bipolar devices for implementing a full BiCMOS buffer, or a drive section containing one NPN and one PNP bipolar transistor for implementing a complementary BiCMOS buffer, may be used with the disclosed compute sections. Figs. 10a-10c illustrate three examples of drive sections which may be utilized in the cell of this invention.

A basic cell described in this specification is shown in Fig. 11 essentially comprising one or more compute sections containing small and medium size transistors and one or more drive sections containing large size MOSFET(s) and/or bipolar transistors. If the driver portion of the cell of Fig. 11 were eliminated and the transistors in the compute section(s) made larger to drive larger loads, the resulting cell would still be very advantageous.

Fig. 12 shows an ASIC 120 which contains array 124 comprised of cells, such as the cell of Figs. 2, 8, and 11, which may or may not be metallized. In this ASIC, the

area of the chip outside of array 124 may contain other circuitry connected to interact with array 124. ASIC 120 may also contain a plurality of arrays 124.

The main differences between the compute section described in this specification and the compute section primarily described in my Application Serial No. 07/524,183, issued as Patent No. 5,055,716, are: 1) the addition of a small size P-channel transistor in each compute section; 2) not requiring that the medium P-channel transistors have less current handling capability than the small N-channel transistor; 3) a reduction in the size of each compute section; and 4) the details of the polysilicon and diffusion preconnections.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects and, therefore, the appended claims are to encompass within their scope also changes and modifications as forward in the true spirit and scope of this invention.

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CLAIMS

I claim:

1. A basic cell for use in mask programmable gate array, said cell comprising:

three or more sizes of N-channel transistors, where size corresponds to channel width; and

three or more sizes of P-channel transistors.

2. The basic cell of Claim 1 wherein said three sizes of N-channel transistors comprise:

one or more small size N-channel transistors;

one or more medium size N-channel transistors; and

one or more large size N-channel transistors; and said three sizes of P-channel transistors comprise:

one or more small size P-channel transistors;

one or more medium size P-channel transistors; and

one or more large size P-channel transistors,

wherein said medium size N-channel and P-channel transistors are at least twice the size of said small size N-channel and P-channel transistors, respectively, and

said large size N-channel and P-channel transistors are larger than said medium size N-channel and P-channel transistors, respectively.

3. A basic cell for use in a mask programmable gate array, said basic cell comprising:

one or more substantially rectangular compute sections and one or more drive sections, said one or more drive sections comprising MOS transistors substantially larger than any MOS transistors in said one or more compute sections.

4. A basic cell for use in a mask programmable gate array, said cell comprising:



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one or more substantially rectangular compute sections and one or more drive sections, said one or more drive sections comprising one or more transistors which are different than transistors in said one or more compute sections, each compute section comprising:

one or more small size N-channel transistors;

one or more medium size N-channel transistors;

one or more small size P-channel transistors; and

one or more medium size P-channel transistors,

said small size N-channel and P-channel transistors having narrower channel widths than said medium size N-channel and P-channel transistors, respectively.

5. The basic cell of Claim 4 wherein said channel widths of said small size N-channel and P-channel transistors are less than approximately one-half the channel widths of said medium size N-channel and P-channel transistors, respectively.

6. A basic cell for use in a mask programmable gate array, said cell comprising one or more compute sections, a compute section comprising:

one or more small size P-channel transistors;

one or more medium size P-channel transistors;

one or more small size N-channel transistors; and

one or more medium size N-channel transistors,

said medium size P-channel transistors having a channel width at least approximately twice the channel width of said small size P-channel transistors, said medium size N-channel transistors



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having a channel width at least approximately twice the channel width of said small size N-channel transistors, and said small size P-channel transistors having a channel width smaller than said small size N-channel transistors,

gates of one of said small size P-channel transistors, one of said medium size P-channel transistors, and one of said medium size N-channel transistors being connected in common by polysilicon,

gates of said small size N-channel transistors being isolated from gates of said small and medium size P-channel transistors and from gates of said medium size N-channel transistors.

7. The basic cell of Claim 6 wherein source regions of said one or more small size P-channel transistors and said one or more medium size P-channel transistors are connected by N-type diffusion.

8. The basic cell of Claim 6 further comprising one or more drive sections, a drive section comprising one or more transistors which are different than transistors in said one or more compute sections.

9. An ASIC containing an array of cells, each of said cells comprising:

three or more sizes of N-channel transistors, where size corresponds to channel width; and

three or more sizes of P-channel transistors.

10. An ASIC containing an array of cells, each of said cells comprising:

one or more substantially rectangular compute sections and one or more drive sections, said one or more drive sections comprising one or more transistors which are different than transistors in



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said one or more compute sections, each compute section comprising:

one or more small size N-channel transistors;

one or more medium size N-channel transistors;

one or more small size P-channel transistors; and

one or more medium size P-channel transistors,

said small size N-channel and P-channel transistors having narrower channel widths than said medium size N-channel and P-channel transistors, respectively.

11. An ASIC containing an array of cells, each of said cells comprising one or more compute sections, a compute section comprising:

one or more small size P-channel transistors;

one or more medium size P-channel transistors;

one or more small size N-channel transistors; and

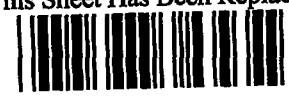
one or more medium size N-channel transistors,

said medium size P-channel transistors having a channel width at least approximately twice the channel width of said small size P-channel transistors, said medium size N-channel transistors having a channel width at least approximately twice the channel width of said small size N-channel transistors, and said small size P-channel transistors having a channel width smaller than said small size N-channel transistors,

gates of one of said small size P-channel transistors, one of said medium size P-channel transistors, and one of said medium size N-channel transistors being connected in common by polysilicon,

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gates of said small size N-channel transistors being isolated from gates of said small and medium size P-channel transistors and from gates of said medium size N-channel transistors.

12. The basic cell of Claim 3 wherein each of said one or more drive sections comprises a plurality of transistors for use as pull-up transistors in a single macrocell and a plurality of transistors for use as pull-down transistors in said single macrocell, said plurality of pull-up and pull-down transistors being programmably connectable so as to provide said macrocell with a variety of output driving capabilities.

13. The basic cell of Claim 3 wherein each of said one or more drive sections comprises one or more transistors for use as pull-up transistors in a single macrocell and a plurality of transistors for use as pull-down transistors in said single macrocell, said plurality of pull-down transistors being programmably connectable so as to provide said macrocell with a variety of output driving capabilities.

14. The basic cell of Claim 3 wherein each of said one or more drive sections comprises a plurality of transistors for use as pull-up transistors in a single macrocell and one or more transistors for use as pull-down transistors in said single macrocell, said plurality of pull-up transistors being programmably connectable so as to provide said macrocell with a variety of output driving capabilities.

15. The basic cell of Claim 4 wherein each of said one or more drive sections comprises a plurality of transistors for use as pull-up transistors in a single macrocell and a plurality of transistors for use as pull-down transistors in said single macrocell, said plurality



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of pull-up and pull-down transistors being programmably connectable so as to provide said macrocell with a variety of output driving capabilities.

16. The basic cell of Claim 4 wherein each of said one or more drive sections comprises one or more transistors for use as pull-up transistors in a single macrocell and a plurality of transistors for use as pull-down transistors in said single macrocell, said plurality of pull-down transistors being programmably connectable so as to provide said macrocell with a variety of output driving capabilities..

17. The basic cell of Claim 4 wherein each of said one or more drive sections comprises a plurality of transistors for use as pull-up transistors in a single macrocell and one or more transistors for use as pull-down transistors in said single macrocell, said plurality of pull-up transistors being programmably connectable so as to provide said macrocell with a variety of output driving capabilities.

18. The basic cell of Claim 10 wherein each of said one or more drive sections comprises a plurality of transistors for use as pull-up transistors in a single macrocell and a plurality of transistors for use as pull-down transistors in said single macrocell, said plurality of pull-up and pull-down transistors being programmably connectable so as to provide said macrocell with a variety of output driving capabilities.

19. The basic cell of Claim 10 wherein each of said one or more drive sections comprises one or more transistors for use as pull-up transistors in a single macrocell and a plurality of transistors for use as pull-



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down transistors in said single macrocell, said plurality of pull-down transistors being programmably connectable so as to provide said macrocell with a variety of output driving capabilities.

20. The basic cell of Claim 10 wherein each of said one or more drive sections comprises a plurality of transistors for use as pull-up transistors in a single macrocell and one or more transistors for use as pull-down transistors in said single macrocell, said plurality of pull-up transistors being programmably connectable so as to provide said macrocell with a variety of output driving capabilities.

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BASIC CELL ARCHITECTURE FOR MASK PROGRAMMABLE GATE ARRAY

Abbas El Gamal

ABSTRACT OF THE DISCLOSURE

A highly efficient CMOS cell structure for use in a metal mask programmable gate array, such as a sea-of-gates type gate array, is disclosed herein. In a basic cell, in accordance with one embodiment of the invention, three or more sizes of N-channel transistors and three or more sizes of P-channel transistors are used. The larger size transistors are incorporated in a drive section of a cell, while the smaller size transistors are incorporated in each compute section of a cell. The particular transistors in the compute and drive sections and the arrangements of the compute and drive sections provide a highly efficient use of silicon real estate while enabling the formation of a wide variety of macrocells to be formed.

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Date of Signature

Signature

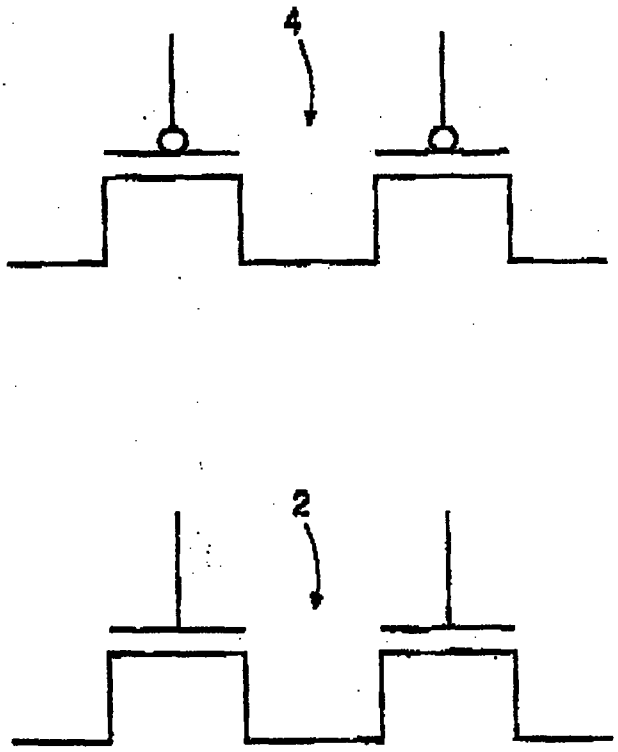


Fig. 1
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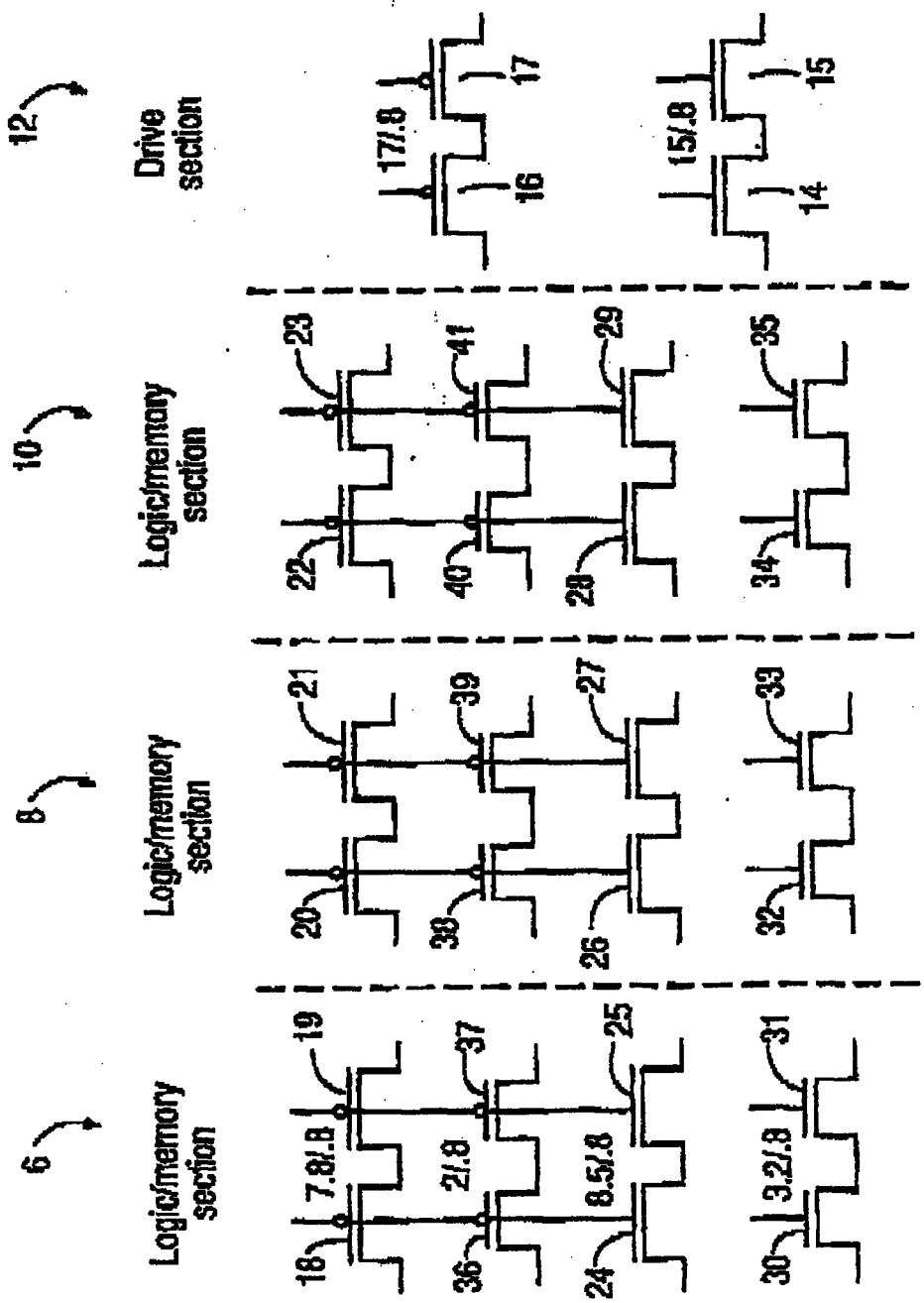

6
Logic/memory section
8
Logic/memory section
10
Logic/memory section
12
Drive section
7.8/.8
2/.8
8.5/.8
3.2/.8
17/.8
15/.8
18
19
36
37
24
25
30
31
20
21
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Fig. 2

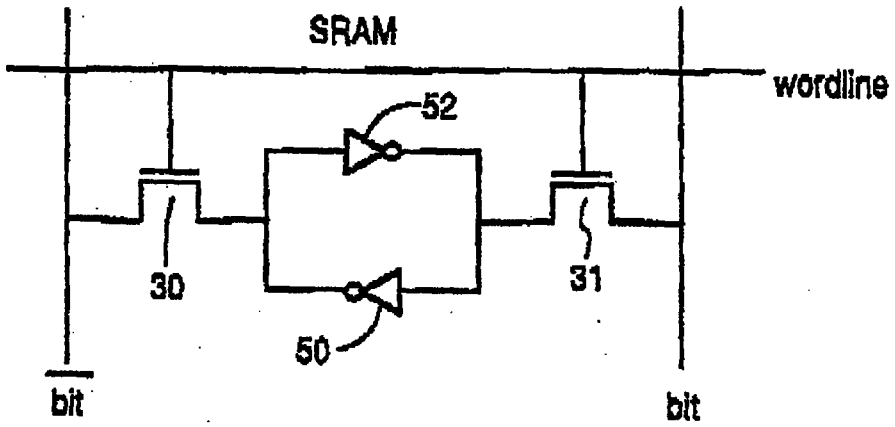


Fig. 3a

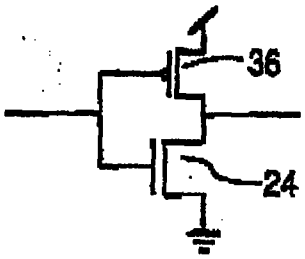


Fig. 3b

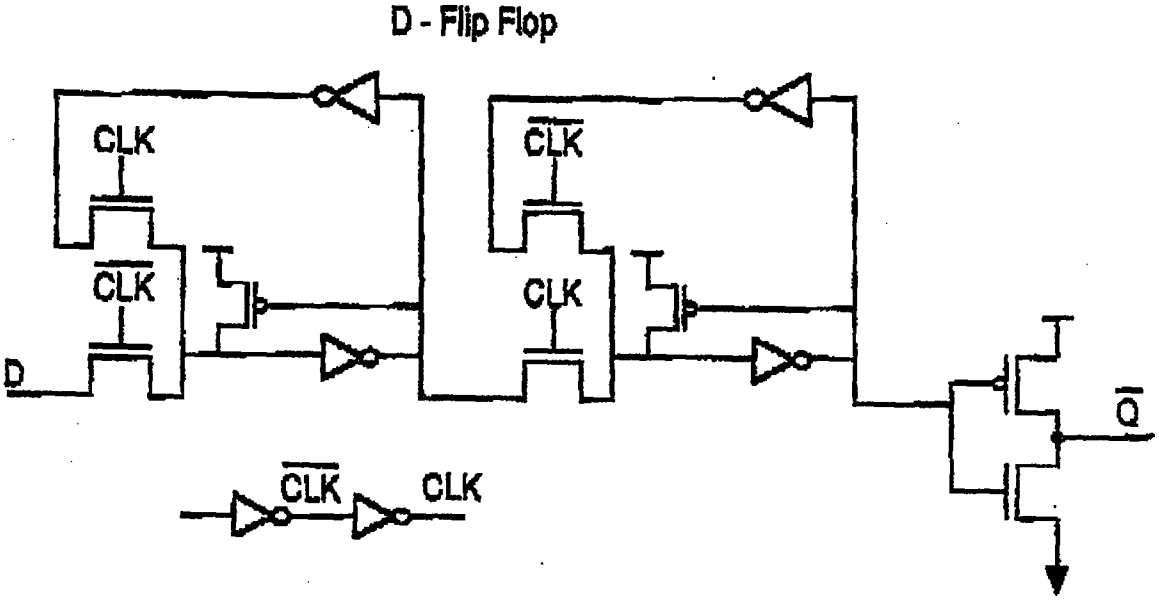


Fig. 4

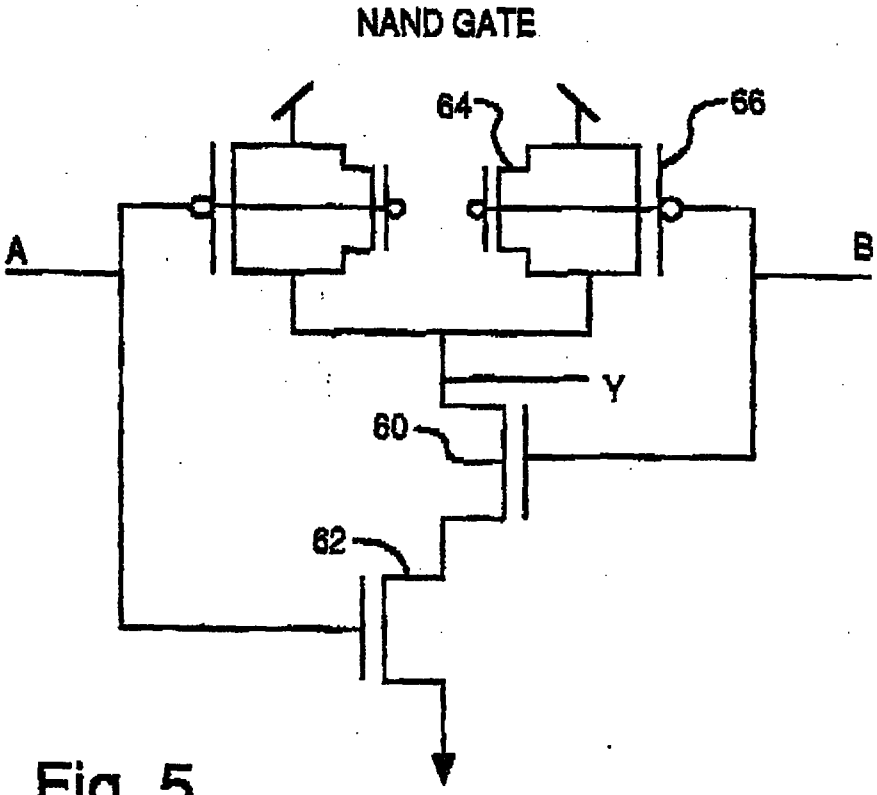


Fig. 5

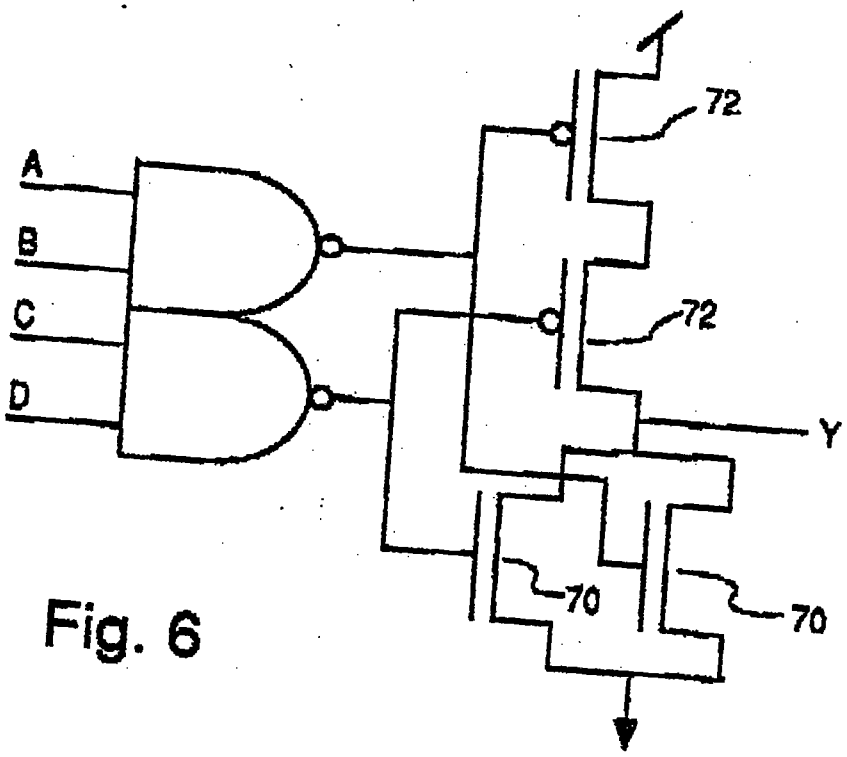


Fig. 6

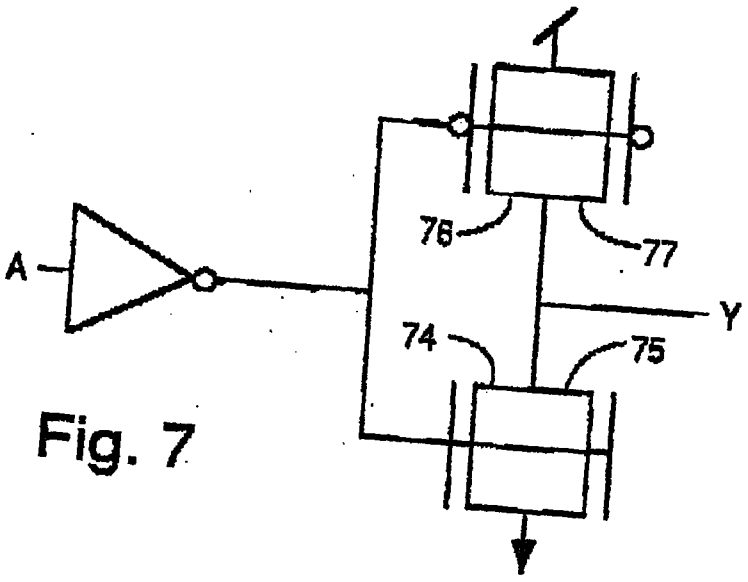


Fig. 7

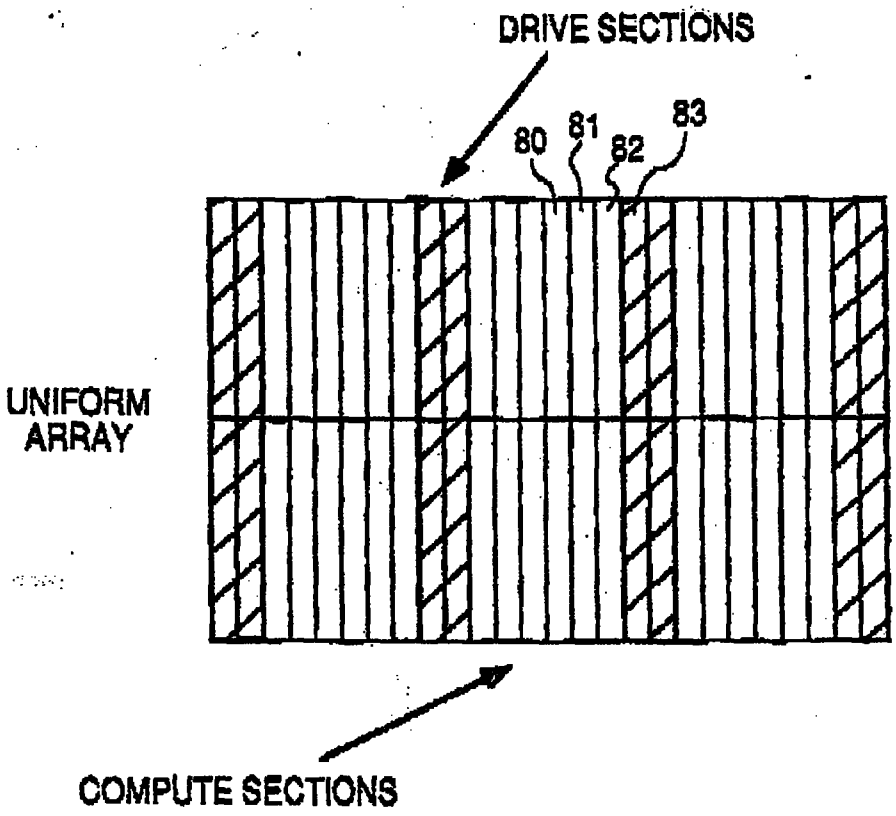

DRIVE SECTIONS
80
81
82
83
UNIFORM ARRAY
COMPUTE SECTIONS

Fig. 8a

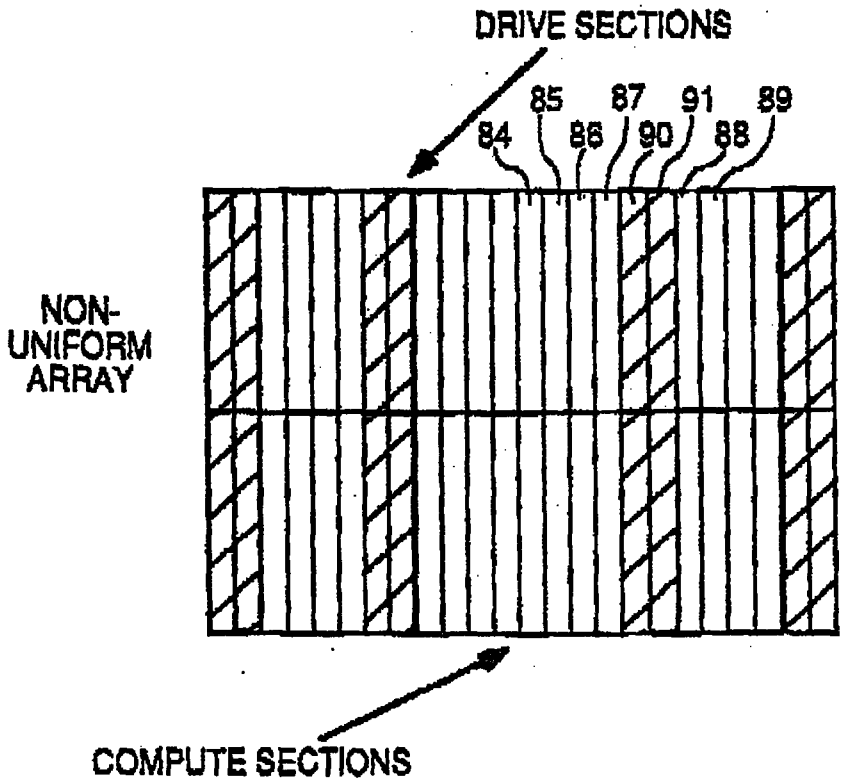

DRIVE SECTIONS
84
85
86
87
90
91
88
89
NON-UNIFORM ARRAY
COMPUTE SECTIONS

Fig.8b

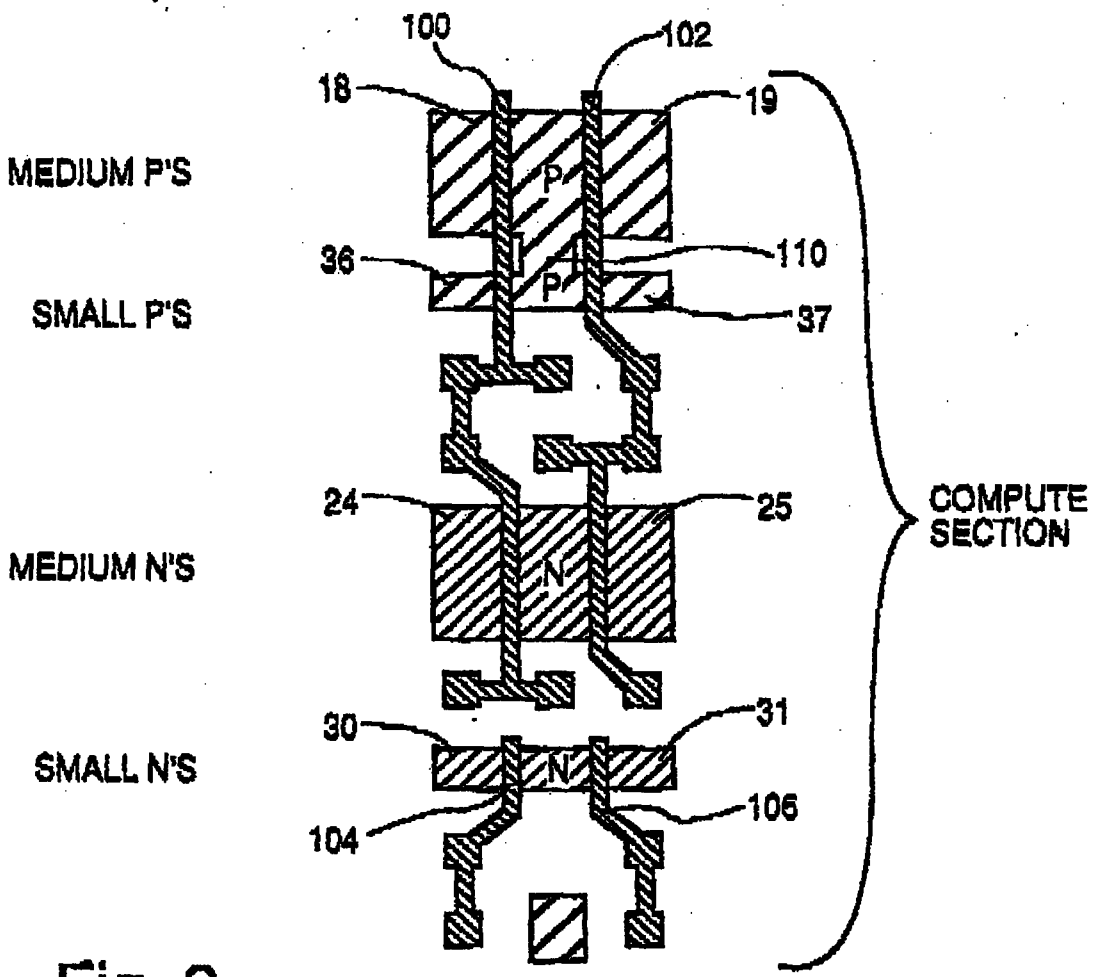


Fig. 9

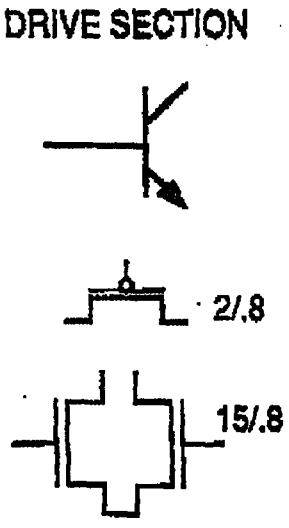


Fig. 10a

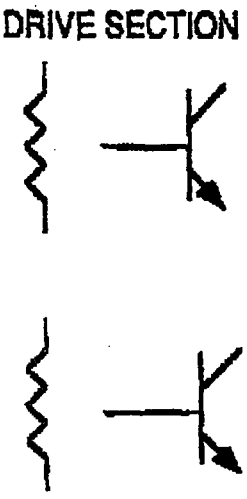


Fig. 10b

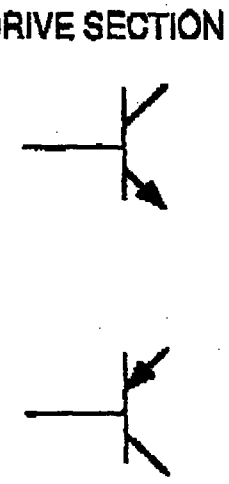


Fig. 10c

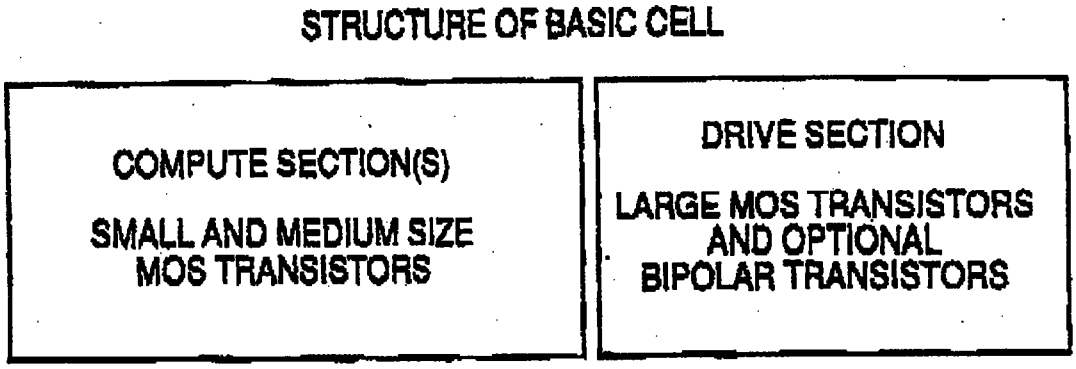

STRUCTURE OF BASIC CELL
COMPUTE SECTION(S)
SMALL AND MEDIUM SIZE MOS TRANSISTORS
DRIVE SECTION
LARGE MOS TRANSISTORS AND OPTIONAL BIPOLAR TRANSISTORS

Fig. 11

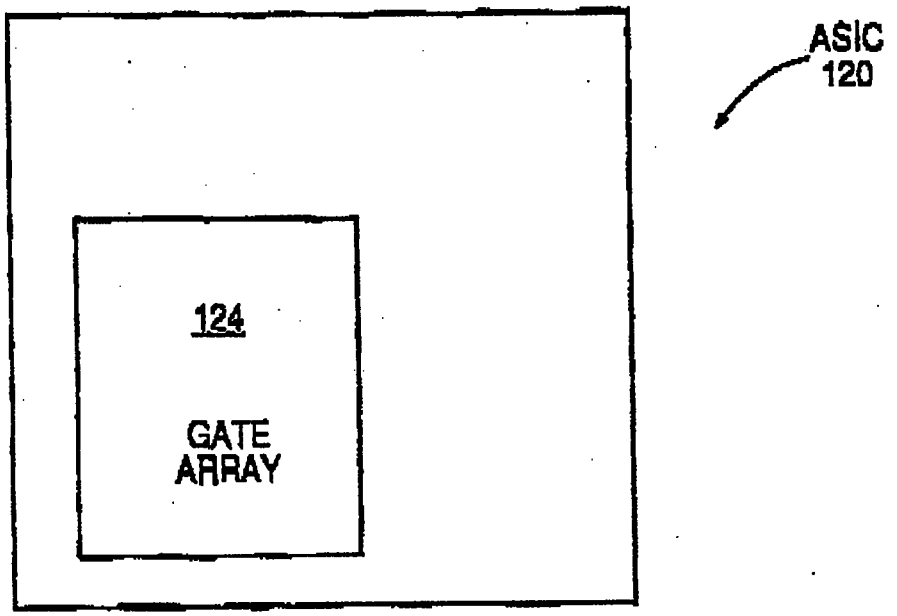

ASIC
120
124
GATE ARRAY

Fig. 12

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BASIC CELL ARCHITECTURE FOR MASK PROGRAMMABLE GATE ARRAY

Abbas El Gamal

ABSTRACT OF THE DISCLOSURE

A highly efficient CMOS cell structure for use in a metal mask programmable gate array, such as a sea-of-gates type gate array, is disclosed herein. In a basic cell, in accordance with one embodiment of the invention, three or more sizes of N-channel transistors and three or more sizes of P-channel transistors are used. The larger size transistors are incorporated in a drive section of a cell, while the smaller size transistors are incorporated in each compute section of a cell. The particular transistors in the compute and drive sections and the arrangements of the compute and drive sections provide a highly efficient use of silicon real estate while enabling the formation of a wide variety of macrocells to be formed.

Figure 2

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CLAIMS

1. A cell comprising:

a compute section or a plurality of substantially identical compute sections, the or each compute section being substantially rectangular and containing MOS transistors for being connected to other transistors; and

a drive section or a plurality of substantially identical drive sections, the or each drive section being substantially rectangular and comprising one or more MOS transistors substantially larger than any MOS transistors in the or each compute section, gates of the or each drive section MOS transistors being isolated from gates of the MOS transistors in the compute section or sections, the or each drive section MOS transistor being for connection to other transistors,

wherein the or each compute section comprises:

two or more small size N-channel transistors, where size corresponds to channel width, at least two of the small size N-channel transistors sharing a common N-type diffused dopant region;

two or more medium size N-channel transistors, at least two of the medium size N-channel transistors sharing a common N-type diffused dopant region;

two or more small size P-channel transistors, at least two of the small size P-channel transistors sharing a common P-type diffused dopant region; and

two or more medium size P-channel transistors, at least two of the medium size P-channel transistors having narrower channel widths than the medium size N-channel and P-channel transistors, respectively,

gates of one or more of the small size N-channel transistors being isolated from gates of the medium size N-channel transistors.

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2. A cell as claimed in claim 1 wherein the medium size N-channel and P-channel transistors are at least twice the size of the small size N-channel and P-channel transistors, respectively.

3. A cell as claimed in claim 1 or 2 wherein a gate of one of the small size P-channel transistors, a gate of one of the medium size P-channel transistors, and a gate of one of the medium size N-channel transistors are formed in common, so as to be connected.

4. A cell as claimed in claim 1, 2 or 3 wherein the or each drive section MOS transistor comprises at least one large size N-channel transistor and at least one large size P-channel transistor, where size corresponds to channel width, the at least one large size N-channel transistor and the at least one large size P-channel transistor having channel widths larger than the respective channel widths of the medium size N-channel and P-channel transistors.

5. A cell as claimed in claim 1, 2 or 3 wherein the one or each drive section MOS transistor comprises at least one large size N-channel transistor, where size correspond to channel width, the at least one large size N-channel transistor having a channel width larger than the respective channel widths of the medium size N-channel transistors, the one or more drive sections also including at least one bipolar transistor for providing pull-up drive capabilities.

6. A cell comprising one or more compute sections, the or each compute section comprising:

one or more small size P-channel transistors, where size corresponds to channel width;

one or more medium size P-channel transistors;

one or more small size N-channel transistors; and

one or more medium size N-channel transistors,

the or each medium size P-channel transistor having a channel width at least approximately twice the

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channel width of the small size P-channel transistor or transistors, the or each medium size N-channel transistor having a channel width at least approximately twice the channel width of the small size N-channel transistor or transistors, and the or each small size P-channel transistors having a channel width smaller than the small size N-channel transistor or transistors,

a gate of one of the small size P-channel transistors, a gate of one of the medium size P-channel transistors, and a gate of one of the medium size N-channel transistors being connected in common by polysilicon,

gates of the small size N-channel transistors being isolated from gates of the small and medium size P-channel transistors and from gates of the medium size N-channel transistors.

7. A cell as claimed in claim 6 wherein source regions of the one or more small size P-channel transistors and the one or more medium size P-channel transistors are connected by P-type diffusion.

8. A cell as claimed in claim 6 or 7 comprising one or more drive sections, the or each drive section comprising one or more transistors which have a larger current drive capability than transistors in the one or more compute sections, and gates of the transistors in the drive sections being isolated from gates of the transistors in the compute sections.

9. A cell as claimed in any one of claims 1-5 and 8 wherein the or each drive section comprises a plurality of transistors for use as pull-up transistors in a single macrocell and a plurality of transistors for use as pull-down transistors in the single macrocell, the plurality of pull-up and pull-down transistors being programmably connectable so as to provide the macrocell with a variety of output driving

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capabilities.

10. A cell as claimed in any one of claims 1-5 and 8 wherein the or each drive section comprises one or more transistors for use as pull-up transistors in a single macrocell and a plurality of transistors for use as pull-down transistors in the single macrocell, the plurality of pull-down transistors being programmably connectable so as to provide the macrocell with a variety of output driving capabilities.

11. A cell as claimed in any one of claims 1-5 and 8 wherein the or each drive section comprises a plurality of transistors for use as pull-up transistors in a single macrocell and one or more transistors for use as pull-down transistors in the single macrocell, the plurality of pull-up transistors being programmably connectable so as to provide the macrocell with a variety of output driving capabilities.

12. A mask programmable gate array including a cell as claimed in any preceding claim prior to interconnection of transistors in the gate array in a programming step.

13. A mask programmable gate array as claimed in claim 12 wherein the cell is one of a plurality of basic cells located within an interior of the gate array.

14. An application specific integrated circuit (ASIC) containing an array of cells, each as claimed in any one of claims 1-11.

15. A cell as claimed in claim 14 wherein the cells are located within an interior of the array.

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resulting macrocells give rise to inefficient chip area utilization and an increase in interconnect length.

Also in the prior art, to improve the efficiency of implementing SRAM cells, CMOS gate array cells with N-channel transistors of two different sizes have been used. The smaller size N-channel transistors are typically less than one third the size of the larger size N-channel transistors. These prior art cells may also incorporate small size P-channel transistors to perform various functions. However, in such cells, the large transistors are still unnecessarily large for driving low fanout nets and inadequate for driving high fanout nets, while the small transistors are inadequate for driving almost all nets. Generally, for these prior art devices to drive high fanout nets, two or more macrocells must be connected in parallel or separate buffers must be introduced.

In the prior art, since the small size transistors used in SRAMs are typically not used for implementing logic macrocells, such as D-flip flops, these logic macrocells are area inefficient. Moreover, the input capacitance for the macrocells is generally unnecessarily high.

According to the present invention, there is provided a mask programmable cell prior to programming comprising: a compute section or a plurality of substantially identical compute sections, the or each compute section being substantially rectangular and containing MOS transistors for being connected to other transistors; and a drive section or a plurality of substantially identical drive sections, the or each drive section being substantially rectangular and comprising one or more MOS transistors having a channel width substantially larger than a channel width of any MOS transistors in the or each compute section, gates of the or each drive section MOS transistors being isolated from gates of the MOS transistors in the compute section or sections, the or

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each drive section MOS transistor being for connection to other transistors, wherein the cell comprises: two or more small size N-channel transistors, where size corresponds to channel width; two or more medium size N-channel transistors, at least two of the medium size N-channel transistors sharing a common N-type diffused dopant region; one or more large size N-channel transistors; two or more small size P-channel transistors; and two or more medium size P-channel transistors, at least two of the medium size P-channel transistors sharing a common P-type diffused dopant region, gates of one or more of the small size N-channel transistors being isolated from gates of the medium size N-channel transistors, a gate of one or more of the medium size P-channel transistors and a gate of one or more of the medium size N-channel transistors being connected together by polysilicon prior to programming said cell.

Thus, a highly efficient CMOS cell structure for use in a metal mask programmable gate array, such as a sea-of-gates type gate array, is disclosed herein. In a basic cell, in accordance with one embodiment of the invention, three or more sizes of N-channel transistors and three or more sizes of P-channel transistors are used. The larger size transistors are incorporated in a drive section of a cell, while the smaller size transistors are incorporated in a compute section of a cell. The larger size transistors may be used for driving high fanout nets and even used to perform logic functions, while the smaller transistors may be used to implement SRAM cells and logic functions and for driving low fanout nets.

The particular transistors in the compute and drive sections, and the arrangements of the transistors in the compute and drive sections, provide a highly efficient use of silicon real estate while enabling the formation of a wide variety of macrocells to be formed.

The invention will now be described, by way of

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example, with reference to the accompanying drawings, in which:

Fig 1 shows a basic prior art cell;

Fig 2 shows a basic cell schematic for a preferred embodiment cell in a mask programmable sea-of-gates structure;

Figs 3a and 3b illustrate an SRAM built using a single compute section of the cell of Fig 2;

Figs 4-7 show various logic circuits or macrocells which may be implemented with the cell structure and array layout shown in Figs 2 and 8;

Figs 8a and 8b illustrate sample tiling of the compute and drive sections in a mask programmable sea of gates structure;

Fig 9 shows a preferred layout for a single compute section in the basic cell structure of Fig 2;

Figs 10a-10c illustrate drive sections which may be used in conjunction with the compute sections of this invention;

Fig 11 illustrates a basic cell in accordance with the invention;

Fig 12 illustrates an ASIC device incorporating a gate array.

The preferred embodiment of the invention is illustrated in Fig 2, where a single mask programmable gate array cell contains one or more compute sections 6, 8, 10 and may contain a drive sections 12 or share a drive section with another cell. The mask programmable gate

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CLAIMS

1. A mask programmable cell prior to programming comprising:

a compute section or a plurality of substantially identical compute sections, the or each compute section being substantially rectangular and containing MOS transistors for being connected to other transistors; and

a drive section or a plurality of substantially identical drive sections, the or each drive section being substantially rectangular and comprising one or more MOS transistors having a channel width substantially larger than a channel width of any MOS transistors in the or each compute section, gates of the or each drive section MOS transistors being isolated from gates of the MOS transistors in the compute section or sections, the or each drive section MOS transistor being for connection to other transistors,

wherein the cell comprises:

two or more small size N-channel transistors, where size corresponds to channel width;

two or more medium size N-channel transistors, at least two of the medium size N-channel transistors sharing a common N-type diffused dopant region;

one or more large size N-channel transistors;

two or more small size P-channel transistors; and

two or more medium size P-channel transistors, at least two of the medium size P-channel transistors sharing a common P-type diffused dopant region,

gates of one or more of the small size N-channel transistors being isolated from gates of the medium size N-channel transistors, a gate of one or more of the medium

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size P-channel transistors and a gate of one or more of the medium size N-channel transistors being connected together by polysilicon prior to programming said cell.

2. A cell as claimed in claim 1 wherein the medium size N-channel and P-channel transistors are approximately equal to or greater than twice the size of the small size N-channel transistors.

3. A cell as claimed in claim 1 or 2 wherein the or each drive section MOS transistor comprises at least one large size N-channel transistor and at least one large size P-channel transistor, where size corresponds to channel width, the at least one large size N-channel transistor and the at least one large size P-channel transistor having channel widths larger than the respective channel widths of the medium size N-channel and P-channel transistors.

4. A cell as claimed in claim 1 or 2 wherein the one or each drive section MOS transistor comprises at least one large size N-channel transistor, where size corresponds to channel width, the at least one large size N-channel transistor having a channel width larger than the respective channel widths of the medium size N-channel transistors, the one or more drive sections also including at least one bipolar transistor for providing pull-up drive capabilities.

5. A cell as claimed in any one of the preceding claims wherein source regions of the one or more medium size P-

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channel transistors are connected by P-type diffusion.

6. A cell as claimed in any one of the preceding claims wherein the or each drive section comprises a plurality of transistors for use as pull-up transistors in a single macrocell and a plurality of transistor for use as pull-down transistors in the single macrocell, the plurality of pull-up and pull down transistors being programmably connectable so as to provide the macrocell with a variety of output driving capabilities.

7. A cell as claimed in any one of claims 1 to 5, wherein the or each drive section comprises one or more transistors for use as pull-up transistors in a single macrocell and a plurality of transistors for use as pull-down transistors in the single macrocell, the plurality of pull-down transistors being programmably connectable so as to provide the macrocell with a variety of output driving capabilities.

8. A cell as claimed in any one of claims 1 to 5, wherein the or each drive section comprises a plurality of transistors for use as pull-up transistors in a single macrocell and one or more transistors for use as pull-down transistors in the single macrocell, the plurality of pull-up transistors being programmably connectable so as to provide the macrocell with a variety of output driving capabilities.

9. A mask programmable gate array including a cell as claimed in any preceding claim prior to interconnection of

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transistors in the gate array in a programming step.

10. A mask programmable gate array as claimed in any preceding claim wherein the cell is one of a plurality of basic cells located within an interior of the gate array.

11. An application specific integrated circuit (ASIC) containing an array of cells, each as claimed in any one of the preceding claims.

12. A cell as claimed in any one of the preceding claims wherein the or each compute section contains said one or more small size P-channel transistors.

13. A cell as claimed in any one of the preceding claims wherein a gate of one of the small size P-channel transistors in connected in common with a gate of one of the medium size P-channel transistors.

14. A cell as claimed in any preceding claim, wherein at least two of said small P-channel transistors share a common P-type diffused dopant region.

15. A cell as claimed in claim 12, 13 or 14, wherein the or each medium size P-channel transistor has a channel width at least approximately twice the channel width of the small size P-channel transistor or transistors, the or each medium size N-channel transistor has a channel width at least approximately twice the channel width of the small size N-channel transistor or transistors, and the or each small size P-channel transistor has a channel width

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smaller than the small size N-channel transistor or transistors.

16. A cell as claimed in any one of the preceding claims as part of an array of cells wherein a drive section of a cell is directly adjacent to a drive section of an adjacent cell so that transistors within drive sections of two adjacent cells can be shared by the adjacent cells.

17. A cell as claimed in any one of the preceding claims wherein said medium size P and N channel transistors are approximately one half the size of said larger MOS transistors in said drive section.

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BASIC CELL ARCHITECTURE FOR MASK PROGRAMMABLE GATE ARRAY

Abbas El Gamal

ABSTRACT OF THE DISCLOSURE

A highly efficient CMOS cell structure for use in a metal mask programmable gate array, such as a sea-of-gates type gate array, is disclosed herein. In a basic cell, in accordance with one embodiment of the invention, three or more sizes of N-channel transistors and three or more sizes of P-channel transistors are used. The larger size transistors are incorporated in a drive section of a cell, while the smaller size transistors are incorporated in each compute section of a cell. The particular transistors in the compute and drive sections and the arrangements of the compute and drive sections provide a highly efficient use of silicon real estate while enabling the formation of a wide variety of macrocells to be formed.

Figure 2

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