TITLE

INTERCONNECTS WITH HARMONIZED STRESS AND METHODS FOR FABRICATING THE SAME

BACKGROUND

The present invention relates to semiconductor features, and in particular to an interconnect for integrated circuits.

Reduction of integrated circuit feature size has resulted in levels of electrically conductive interconnects being placed closer together vertically, as well as reduction of the horizontal spacing between the electrically conductive interconnects, such as metal lines. As a result, capacitance has increased between such conductive portions, resulting in RC (resistance x conductance) delay time and crosstalk effect. One proposed approach to this problem is to replace the conventional silicon oxide (SiO_2) dielectric material, having a dielectric constant (k) of about 4.0, with other insulation material having a lower dielectric constant, to thereby lower capacitance.

Unfortunately, low-k dielectric materials have various problems that make integration into existing integrated circuit structures and processes difficult. Compared to conventional dielectric materials used in semiconductor fabrication, most low-k materials typically present characteristics such as high tensile stress. Such high tensile stresses accumulating in a semiconductor structure can lead to bowing or deformation, cracking, peeling, or formation of voids of a film therein, which can damage or destroy an interconnect that includes the film, affecting reliability of a resulting integrated circuit.

SUMMARY

Therefore, there is a need for an interconnect for integrated circuits with improved stress harmonization.

Interconnects with harmonized stress and methods for fabricating the same are provided. An exemplary embodiment of an interconnect comprises a substrate having a conductive member. A composite low-k dielectric layer interposed with at least one stress-harmonizing layer therein overlies the substrate. A conductive feature formed in the composite

low-k dielectric layer passes through the at least one stress-harmonizing layer to electrically connect the conductive member.

An exemplary embodiment of a dual damascene structure comprises a substrate having a conductive member. A composite low-k dielectric layer interposed with at least one stress-harmonizing layer overlies the substrate. A conductive feature formed in the composite low-k dielectric layer passes through the at least one stress-harmonizing layer to electrically connect the conductive member, wherein the conductive feature comprises an underlying conductive via and an overlying conductive line stacked thereon.

An exemplary embodiment of a method for fabricating an interconnect with harmonized stress comprises providing a substrate with a conductive member thereon. A composite low-k dielectric layer interposed with at least one stress-harmonizing layer therein is formed to overlie the substrate. An opening is formed in the composite low-k dielectric and passes through the stress-harmonizing layer to expose a portion of the conductive member. The opening

is filled with conductive material to form a conductive feature electrically connecting the conductive member.

A detailed description is given in the following embodiments with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention can be more fully understood by reading the subsequent detailed description and examples with reference made to the accompanying drawings, wherein:

Figs. 1-4 are cross sections of a portion of a substrate during fabrication of an interconnect with harmonized stress, according to an exemplary embodiment of the invention; and

Figs. 5-6 are schematic diagrams showing cross sections of interconnects with harmonized stress, according to various exemplary embodiments of the invention.

DESCRIPTION

Interconnects with harmonized stress and methods for fabricating the same are now described here in greater detail. Some embodiments of the invention, such as the exemplary embodiments describe, can potentially provide

interconnects with dielectric layers with harmonized stress. In some embodiments, this can be accomplished by interposing at least one stress-harmonizing layer between dielectric layers of an interconnect, wherein the stress-harmonizing layer surrounds adjacent conductive features of an interconnect and preferably doesn't contact with a bottom or top surface of the adjacent conductive features.

In this specification, expressions such as "overlying the substrate", "above the layer", or "on the film" simply denote a relative positional relationship with respect to the surface of the base layer, regardless of the existence of intermediate layers. Accordingly, these expressions may indicate not only the direct contact of layers, but also, a non-contact state of one or more laminated layers. By use of the term "low dielectric constant" or "low-k" herein, is meant a dielectric constant (k value) less than the dielectric constant of a conventional silicon oxide. Preferably, the dielectric constant of the low-k is less than about 4.0.

Figs. 1-4 are cross sections of a portion of a substrate during fabrication of an interconnect with harmonized stress according to an exemplary embodiment.

In Fig. 1, a semiconductor substrate 100, for example a silicon substrate, with semiconductor devices or other existing conductive lines thereon is first provided. The substrate 100 is illustrated as a flat substrate here for simplicity. As shown in Fig. 1, the semiconductor substrate 100 is also provided with a conductive member 102 electrically connecting one of the underlying semiconductor devices or conductive lines (both not shown).

Next, low-k dielectric layers 104 and 108 of a first type stress and a stress-harmonizing layer 106 of a second type stress are then alternatively formed over the substrate 100 and the conductive member 102. Normally, the first type stress of the low-k dielectric layers shows tensile stress and the second type stress of the stress-harmonizing layer 106 shows a compressive stress contrary to the first type stress. The low-k dielectric layers 104 and 108 may comprise dielectric materials such as carbon-doped silicon dioxide materials, fluorinated silicate glass (FSG), organic

silicate glass (OSG), fluorine doped silicon oxide, spin-on glasses, silsesquioxane, benzocyclobutene (BCB)-based polymer dielectrics and any silicon containing low-k dielectric. Low-k dielectric layers 104 and 108 are formed at a thickness of about 100-3000 Å, and 100-5000 Å, respectively. Stress-harmonizing layer 106 is formed at a thickness of about 200-1000 Å. to thereby provide a compressive stress of about 50-550 MPa to thereby harmonize tensile stresses provided by the overlying and underlying low-k dielectric layers (referring to low-k dielectric layers 104 and 108). Therefore, bowing or deformation of the composite film 110 illustrated in Fig. 1 is thus prevented and cracking, peeling, or formation of voids in the composite film 110 can also be reduced. The stress-harmonizing layer 106 may comprise dielectric materials such as oxide, oxynitride, silicon carbide, nitride, silicon carbine containing oxygen ($Si_aC_bO_c$), or silicon carbine containing nitrogen ($Si_xC_yN_z$), wherein a, b, c, x, y, z are formed at about 0.8-1.2 , 0.8-1.2 , 0-0.8, 0.8-1.2, 0.8-1.2, and 0-0.6, respectively. Preferably, the stress-harmonizing layer 106 comprises silicon carbine containing oxygen

($Si_aC_bO_c$), silicon carbine containing nitrogen ($Si_xC_yN_z$), and nitride. The stress-harmonizing layer 106 can be formed by, for example, plasma enhanced chemical vapor deposition (PECVD) and can be in-situ formed during formation of one or both of the low-k dielectric layers 104 and 108 or ex-situ formed by additional deposition.

In Fig. 2, an opening 112, for example a dual damascene opening having a lower via portion 112a and an upper trench portion 112b, is then formed through the low-k dielectric layers 104, 108, and the stress-harmonizing layer 106 using a known dual damascene process of either trench first formed or via first formed. The lower via portion 112a of the opening 112 exposes a portion of the underlying conductive member 102.

The opening 112 can be formed by sequential photolithography and etching steps, wherein the etching step may be a time mode etching utilizing adequate etching chemistries to thereby reduce the use of an etch stop layer (ESL) conventionally disposed between the composite dielectric layer 110 and the substrate 100, and in the low-k dielectric layer 108 of the composite dielectric layer 110.

Therefore, elevation of the overall dielectric constant of the composite layer 110 can be prevented.

In Fig. 3, a diffusion barrier layer 114 is conformably formed in the opening 112 and over the low-k dielectric layer 108. The diffusion barrier layer 114 may comprise conductive material such as titanium (Ti), tantalum (Ta), titanium nitride (TiN), tantalum nitride (TaN), or combinations thereof. Normally, the diffusion barrier layer 114 is formed at a thickness of about 20-200 Å. Next, a conductive layer 116 of a conductive material such as copper or copper alloy is then formed in the opening 110 and over the low-k dielectric layer 108. The conductive layer 116 can be formed by known electrochemical plating (ECP) when utilizing copper or copper alloy as conductive material therein.

In Fig. 4, the portion of the diffusion barrier 114 and the conductive layer 116 over the opening 112 are then removed by, for example, chemical mechanical polishing (CMP), such that an interconnect with a planar surface remains. Next, an additional conductive cap 118 is selectively formed over the conductive layer 116, providing

encapsulation thereof from the top. The conductive cap 118 can be selectively formed by, for example, electroless plating and may comprise conductive materials such as cobalt tungsten (CoW), cobalt phosphorus (CoP), or cobalt tungsten phosphorus (CoWP). The conductive cap 118 can be formed at a thickness of about 20-200 Å. Therefore, a conductive feature S is formed and undesired interlayer ion diffusion to the adjacent low-k dielectric layers from the conductive material, for example copper or copper alloy, of the conductive feature S can be thus eliminated or prevented. An interconnect with harmonized stress is thus formed.

Next, a dielectric layer 120 such as a low-k dielectric layer is formed over the low-k dielectric layer 108 and the conductive feature S. Sequential processes can be further performed on the dielectric layer 120 to thereby complete the integrated circuit fabrication.

In an exemplary embodiment, the interconnect is illustrated as a dual damascene structure with a conductive feature S having a conductive plug and a conductive line. The stress-harmonizing layer 106 formed in the dual damascene structure can harmonize the tensile stresses

within the interconnect mainly provided by the low-k dielectric layers.

Moreover, numbers and locations of the stress-harmonizing layer 106 may vary. For example, the stress-harmonizing layer 106 may be located elsewhere than illustrated in Fig. 4. The stress-harmonizing layer 106 can be formed in the low-k dielectric layer 108 surrounding the upper trench portion 112a, as shown in Fig. 5. In addition, more than one stress-harmonizing layer (referring to the stress-harmonizing layer 106a-c) can be formed at various positions in the composite layer 110, surrounding the conductive feature S, as shown in Fig. 6.

Since there is no need for additional etch stop layers for the interconnect, the stress-harmonizing layer 106 is preferably formed at a distance from the topmost or bottommost surface of the conductive feature S for ease of fabrication.

In addition, if the etch stop layer is desired, the stress-harmonizing layer 106 may be formed at a distance from the junction of the via portion 112a and the trench

portion 112b of the opening 112, thereby providing locations for formation of such etch stop layer.

In the above exemplary embodiments, the interconnects are illustrated as a dual damascene structure. It will be understood by those skilled in the art that the invention can be also applied to a single damascene structure which is not discussed here for simplicity.

As shown In Fig. 4, an embodiment of an interconnect with harmonized stress is illustrated. The interconnect includes a substrate having a conductive member. A composite low-k dielectric layer interposed with at least one stress-harmonizing layer therein overlies the substrate. A conductive feature formed in the composite low-k dielectric layer passes through the at least one stress-harmonizing layer to electrically connect the conductive member.

In the above exemplary embodiments, tensile stresses provided by the low-k dielectric layers of an interconnect are harmonized by formation of at least one stress-harmonizing layer with compress stress, preventing problems such as those occurring in a damascene structure when

utilizing low-k dielectric, while improving reliability of the interconnect.

Moreover, the top surface of the conductive feature S in the interconnect can be encapsulated by a conductive cap layer to reduce need for uses of etch stop layers, with factors such as electro-migration (EM) performance of the interconnect thus ensured. The interconnect without etch stop layer is thus obtained with simplified fabrication and low cost.

While the invention has been described by way of example and in terms of preferred embodiment, it is to be understood that the invention is not limited thereto. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A method for forming an interconnect, comprising:

providing a substrate with a conductive member thereon;

forming a composite low-k dielectric layer interposed with at least one stress-harmonizing layer therein overlying the substrate;

forming an opening in the composite low-k dielectric, passing through the stress-harmonizing layer and exposing a portion of the conductive member; and

filling the opening with conductive material to form a conductive feature, electrically connecting the conductive member.

2. The method of claim 1, wherein formation of the composite low-k dielectric layer interposed with at least one stress-harmonizing layer therein comprises:

(a) forming a first layer of low-k dielectric over the substrate;

(b) forming a stress-harmonizing layer over the first layer of low-k dielectric; and

(c) forming a second layer of low-k dielectric over the first stress-harmonizing layer.

3. The method of claim 2, further comprising repeating the steps (a)-(c) for at least once to form a composite low-k dielectric layer interposed with a plurality of stress-harmonizing layers.

4. The method of claim 2, wherein first and the second low-k dielectric layers comprise tensile stress and the first stress-harmonizing layer comprises compressive stress.

5. The method of claim 2, wherein steps (A)-(C) are performed in-situ by plasma-enhanced chemical vapor deposition.

6. The method of claim 1, wherein the at least one stress-harmonizing layer comprises oxide, oxynitride, silicon carbide, nitride, silicon carbine containing oxygen ($Si_aC_bO_c$), or silicon carbine containing nitrogen ($Si_xC_yN_z$).

7. The method of claim 1, wherein the at least one stress-harmonizing layer is formed at a thickness of about 200-1000 Å.

8. The method of claim 1, wherein the at least one stress-harmonizing layer comprises a compressive stress of about 50-350 MPa.

9. The method of claim 1, wherein the at least one stress-harmonizing layer does not contact the substrate or the top surface of the composite low-k dielectric layer.

10. An interconnect, comprising:

a substrate having a conductive member;

a composite low-k dielectric layer interposed with at least one stress-harmonizing layer therein overlying the substrate; and

a conductive feature in the composite low-k dielectric layer, passing through the at least one stress-harmonizing layer and electrically connecting the conductive member.

11. The interconnect of claim 10, wherein the composite low-k dielectric layer comprises a plurality of low-k dielectric portions of tensile stress interleaved with at least one stress-harmonizing layer of compressive stress.

12. The interconnect of claim 10, further comprising a conductive cap selectively formed on the top surface of the conductive feature.

13. The interconnect of claim 10, wherein the at least one stress-harmonizing layer comprises oxide, oxynitride, silicon carbide, nitride, silicon carbine

containing oxygen ($Si_aC_bO_c$), or silicon carbine containing nitrogen ($Si_xC_yN_z$).

14. The interconnect of claim 10, wherein the at least one stress-harmonizing layer is formed at a thickness of about 200-1000 Å.

15. The interconnect of claim 10, wherein the at least one stress-harmonizing layer comprises a compressive stress of about 50-550 MPa.

16. interconnect of claim 10, wherein the at least one stress-harmonizing layer does not contact the substrate or the top surface of the composite low-k dielectric layer.

17. A dual damascene structure, comprising:

a substrate having a conductive member;

a composite low-k dielectric layer interposed with at least one stress-harmonizing layer overlying the substrate; and

a conductive feature in the composite low-k dielectric layer, passing through the at least one stress-harmonizing layer and electrically connecting the conductive member, wherein the conductive feature comprises an underlying conductive via and an overlying conductive line stacked thereon.

18. The dual damascene structure of claim 17, wherein the conductive feature comprises copper or copper alloy.

19. The dual damascene structure of claim 17, wherein the composite low-k dielectric layer comprises a plurality of low-k dielectric portions of tensile stress interleaved with at least one stress-harmonizing layer of compressive stress.

20. The dual damascene structure of claim 17, wherein the at least one stress-harmonizing layer comprises oxide, oxynitride, silicon carbide, nitride,

silicon carbine containing oxygen ($Si_aC_bO_c$), or silicon carbine containing nitrogen ($Si_xC_yN_z$).