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(71) Applicant *(for all designated States except US)*: **QUALCOMM INCORPORATED** [US/US]; 5775 Morehouse Drive, San Diego, CA 92121 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **AHMED, Muhammad** [US/US]; 12340 Alameda Trace Circle #2204, Austin, TX 78727 (US). **PLONDKE, Erich** [US/US]; 12012 Carmel Park Lane, Austin, TX 78727 (US). **CODRESCU, Lucian** [US/US]; 12505 Glacier Parke Cove, Austin, TX 78726 (US). **ANDERSON, William C.** [US/US]; 2800 Waymaker Way #46, Austin, TX 78746 (US).

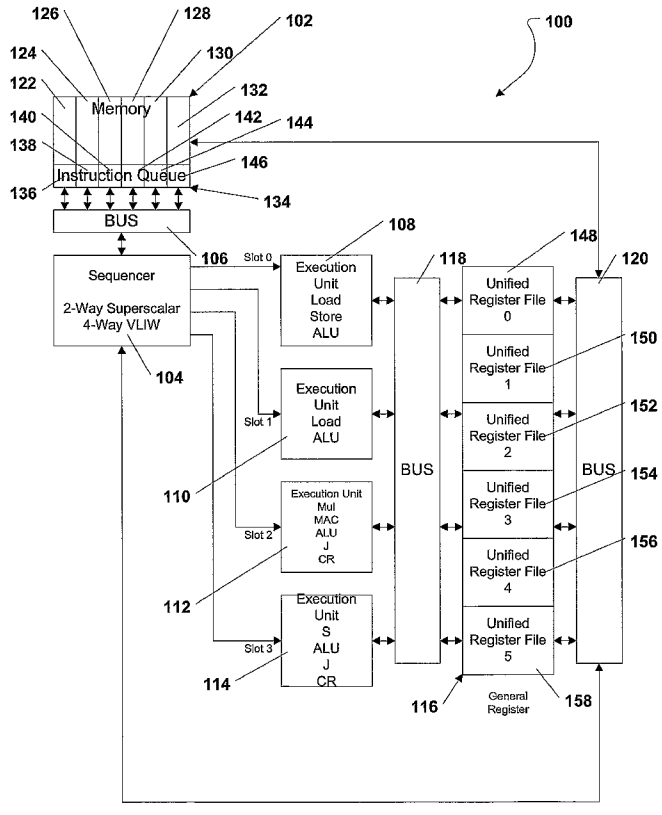
(74) Agents: **WADSWORTH, Philip, R.** et al.; 5775 Morehouse Drive, San Diego, CA 92121 (US).

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(54) Title: SYSTEM AND METHOD OF USING A PREDICATE VALUE TO ACCESS A REGISTER FILE



(57) Abstract: A processor device is disclosed and includes a memory unit and at least one interleaved multi-threading instruction pipeline. The interleaved multi-threading instruction pipeline utilizes a number of clock cycles that is less than an instruction issue rate for each of a plurality of program threads that are stored within the memory unit. The memory unit includes six instruction caches. Further, the processor device includes six register files and each of the six register files is associated with one of the six instruction caches. Each of the plurality of program threads is associated with one of the six register files. Further, each of the six program threads includes a plurality of instructions and each of the plurality of instructions is stored within one of the six instruction caches of the memory.

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