CLAIMS

What is claimed is:

1. An electronic package, comprising:

an interposer, wherein a cavity passes through the interposer;

a nested component in the cavity; and

a die coupled to the interposer by a first interconnect and coupled to the nested component by a second interconnect, wherein the first and second interconnects comprise:

a first bump;

a bump pad over the first bump; and

a second bump over the bump pad.

2. The electronic package of claim 1, wherein the bump pad of the first interconnect is substantially coplanar to the bump pad of the second interconnect.

3. The electronic package of claim 1, wherein the nested component and the interposer are embedded in an underfill layer and a first mold layer.

4. The electronic package of claim 3, wherein the die is embedded in a second mold layer.

5. The electronic package of claim 1, wherein the cavity is entirely within a footprint of the die.

6. The electronic package of claim 1, wherein a first portion of the cavity is within a footprint of the die, and wherein a second portion of the cavity is outside of the footprint of the die.

7. The electronic package of claim 1, wherein through component vias extend through the nested component.

8. The electronic package of claim 1, wherein the nested component is a passive component.

9. The electronic package of claim 1, wherein the nested component is an active component.

10. The electronic package of claim 1, further comprising:

a second die, wherein the second die is coupled to the nested component by a third interconnect comprising:

a first bump;

a bump pad over the first bump; and

a second bump over the bump pad.

11. The electronic package of claim 10, wherein the nested component electrically couples the first die to the second die.

12. The electronic package of claim 1, further comprising:

a second nested component in the cavity.

13. The electronic package of claim 1, wherein an active surface of the nested component faces away from the die.

14. The electronic package of claim 1, wherein the nested component comprises a plurality of stacked dies.

15. The electronic package of claim 1, wherein the interposer comprises a plurality of discrete interposer substrates, wherein edges of the plurality of discrete interposer substrates define the cavity.

16. The electronic package of claim 1, wherein the interposer comprises glass, ceramic, silicon, or organic materials.

17. The electronic package of claim 1, further comprising one or more redistribution layers, wherein the one or more redistribution layers are located over a top surface of the interposer, over a bottom surface of the interposer, over a top surface of the nested component, over a bottom surface of the nested component, over a mold layer that embeds the interposer and the nested component, and/or between the first bumps and the second bumps.

18. An electronic system, comprising:

a board;

a package substrate electrically coupled to the board;

an interposer electrically coupled to the package substrate, wherein the interposer comprises a cavity;

a nested component in the cavity, wherein the nested component is electrically coupled to the package substrate;

a first die electrically coupled to the interposer and the nested component by interconnects; and

a second die electrically coupled to the interposer and the nested component by interconnects, wherein the interconnects comprise:

a first bump;

a bump pad over the first bump; and

a second bump over the bump pad.

19. The electronic system of claim 18, wherein the nested component electrically couples the first die to the second die.

20. The electronic system of claim 18, wherein the nested component is a passive component.

21. The electronic system of claim 18, wherein the nested component is an active component.

22. The electronic system of claim 18, wherein the nested component comprises a plurality of stacked dies.

23. A method of forming an electronic package, comprising:

forming first bump pads and second bump pads on a first carrier, wherein first bumps are disposed over the first bump pads and the second bump pads;

attaching an interposer to the first bump pads, wherein the interposer comprises a cavity;

attaching a nested component to the second bump pads, wherein the nested component is within the cavity of the interposer;

applying a mold layer over the interposer and the nested component;

attaching a second carrier to the mold layer;

removing the first carrier;

exposing surfaces of the first bump pads and the second bump pads opposite from the first bumps; and

attaching a die to the first bump pads and the second bump pads with second bumps.

24. The method of claim 23, further comprising:

applying a second mold layer over the die; and

removing the second carrier.

~~25. The method of claim 24, further comprising:~~

~~attaching interconnects to the interposer and the nested component.~~

CLAIMS:

1. An electronics package, comprising:

an interposer comprising silicon, the interposer comprising vias that provide connections between pads on a bottom of the interposer and a redistribution layer on a top of the interposer;

a first die over the interposer, the first die coupled to the redistribution layer of the interposer by first interconnects;

a second die over the interposer and laterally spaced apart from the first die, the second die coupled to the redistribution layer of the interposer by second interconnects;

a first mold layer between the first die and the interposer and between the second die and the interposer, the first mold layer laterally between and in contact with the first die and the second die, and the first mold layer in contact with the first interconnects and with the second interconnects;

bumps on the pads on the bottom of the interposer and vertically beneath the vias of the interposer, the bumps vertically beneath the first die and vertically beneath the second die; and

a second mold layer beneath the interposer and in contact with a side of the interposer, the second mold layer in contact with the bumps and with the pads on the bottom of the interposer.

2. The electronics package of claim 1, wherein the first mold layer has an uppermost surface at a same level as an uppermost surface of the first die.

3. The electronics package of claim 2, wherein the uppermost surface of the first mold layer is at a same level as an uppermost surface of the second die.

4. The electronics package of claim 1, wherein the second mold layer is in contact with a second side of the interposer, the second side laterally opposite the side.

5. The electronics package of claim 4, wherein the second mold layer is in contact with less than an entirety of the side of the interposer, and with less than an entirety of the second side of the interposer.

6. The electronics package of claim 1, wherein the second mold layer has an edge in vertically alignment with an edge of the first mold layer.

7. The electronics package of claim 1, further comprising:

an underfill material between the interposer and the first mold layer.

8. A method of fabricating an electronics package, the method comprising:

coupling a first die to a redistribution layer of an interposer with first interconnects, the interposer comprising vias that provide connections between pads on a bottom of the interposer and the redistribution layer on a top of the interposer;

coupling a second die to the redistribution layer of the interposer with second interconnects;

forming a first mold layer between the first die and the interposer and between the second die and the interposer, the first mold layer laterally between and in contact with the first die and the second die, and the first mold layer in contact with the first interconnects and with the second interconnects;

forming bumps on the pads on the bottom of the interposer and vertically beneath the vias of the interposer, the bumps vertically beneath the first die and vertically beneath the second die; and

forming a second mold layer beneath the interposer and in contact with a side of the interposer, the second mold layer in contact with the bumps and with the pads on the bottom of the interposer.

9. The method of claim 8, wherein the first mold layer has an uppermost surface at a same level as an uppermost surface of the first die.

10. The method of claim 9, wherein the uppermost surface of the first mold layer is at a same level as an uppermost surface of the second die.

11. The method of claim 8, wherein the second mold layer is in contact with a second side of the interposer, the second side laterally opposite the side.

12. The method of claim 11, wherein the second mold layer is in contact with less than an entirety of the side of the interposer, and with less than an entirety of the second side of the interposer.

13. The method of claim 8, wherein the second mold layer has an edge in vertically alignment with an edge of the first mold layer.

14. The method of claim 8, further comprising:

forming an underfill material between the interposer and the first mold layer.

15. An electronic system, comprising:

a board;

a package substrate coupled to the board; and

an electronics package coupled to the package substrate, the electronics package comprising:

an interposer comprising silicon, the interposer comprising vias that provide connections between pads on a bottom of the interposer and a redistribution layer on a top of the interposer;

a first die over the interposer, the first die coupled to the redistribution layer of the interposer by first interconnects;

a second die over the interposer and laterally spaced apart from the first die, the second die coupled to the redistribution layer of the interposer by second interconnects;

a first mold layer between the first die and the interposer and between the second die and the interposer, the first mold layer laterally between and in contact with the first die and the second die, and the first mold layer in contact with the first interconnects and with the second interconnects;

bumps on the pads on the bottom of the interposer and vertically beneath the vias of the interposer, the bumps vertically beneath the first die and vertically beneath the second die; and

a second mold layer beneath the interposer and in contact with a side of the interposer, the second mold layer in contact with the bumps and with the pads on the bottom of the interposer.

16. The electronic system of claim 15, further comprising:

a battery coupled to the board.

17. The electronic system of claim 15, further comprising:

a camera coupled to the board.

18. The electronic system of claim 15, further comprising:

a display coupled to the board.

19. The electronic system of claim 15, further comprising:

a GPS coupled to the board.

20. The electronic system of claim 15, further comprising:

a communication chip coupled to the board.