Fig. 1

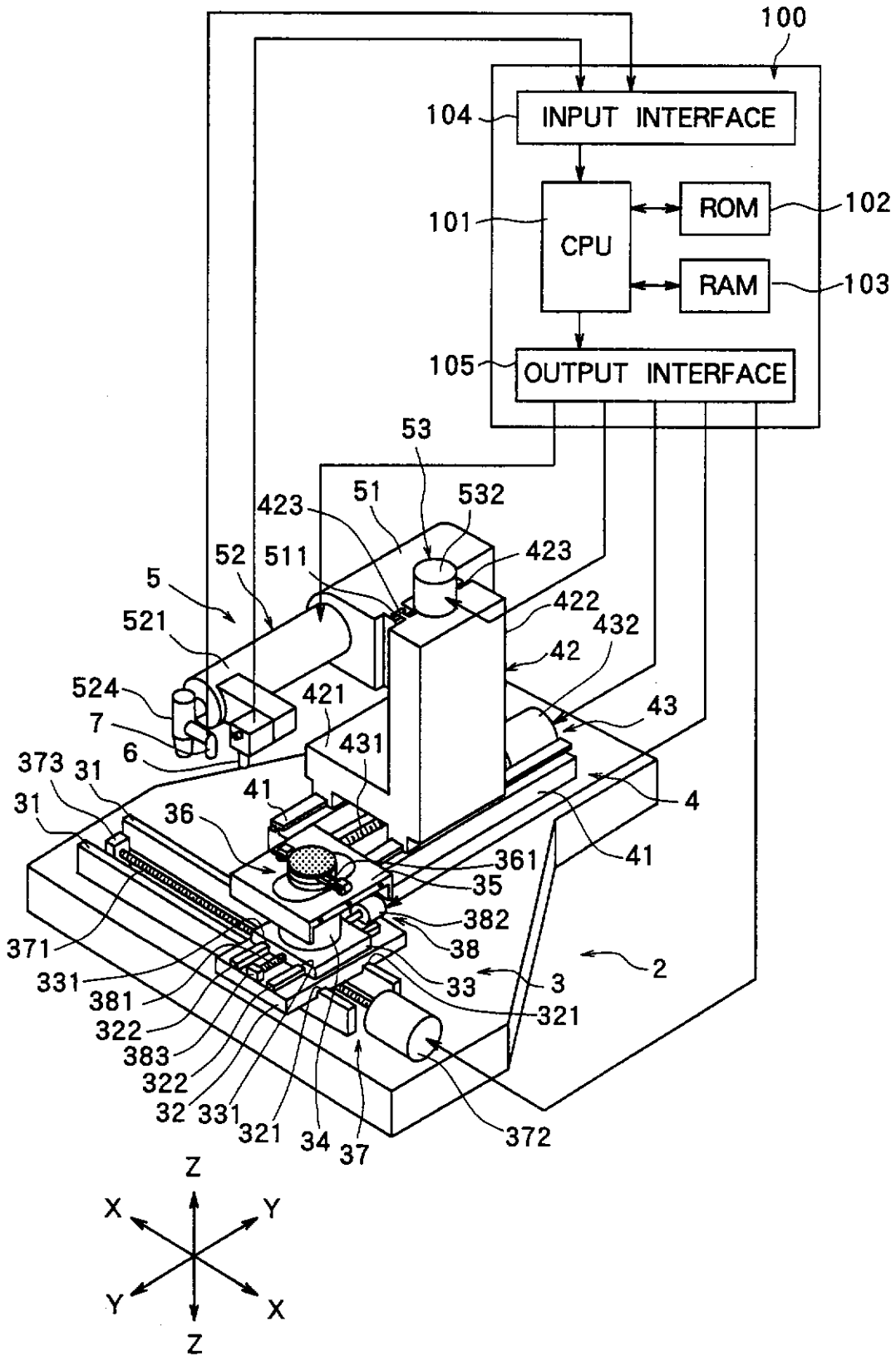

100
104
INPUT INTERFACE
101
CPU
ROM
102
RAM
103
105
OUTPUT INTERFACE
53
51
532
423
52
511
423
5
422
521
432
42
524
421
43
7
431
6
373
31
41
4
31
36
361
41
35
382
371
38
2
331
33
3
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322
383
322
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331
321
34
37
372
Z
X
Y
Y
X
Z

Fig. 2

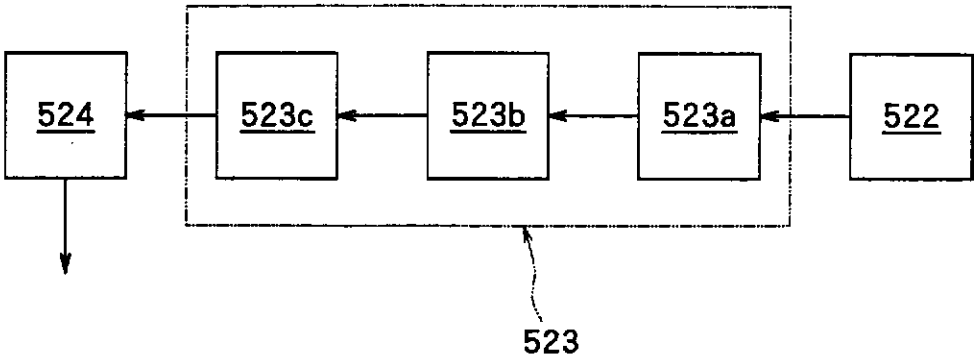


Fig. 3

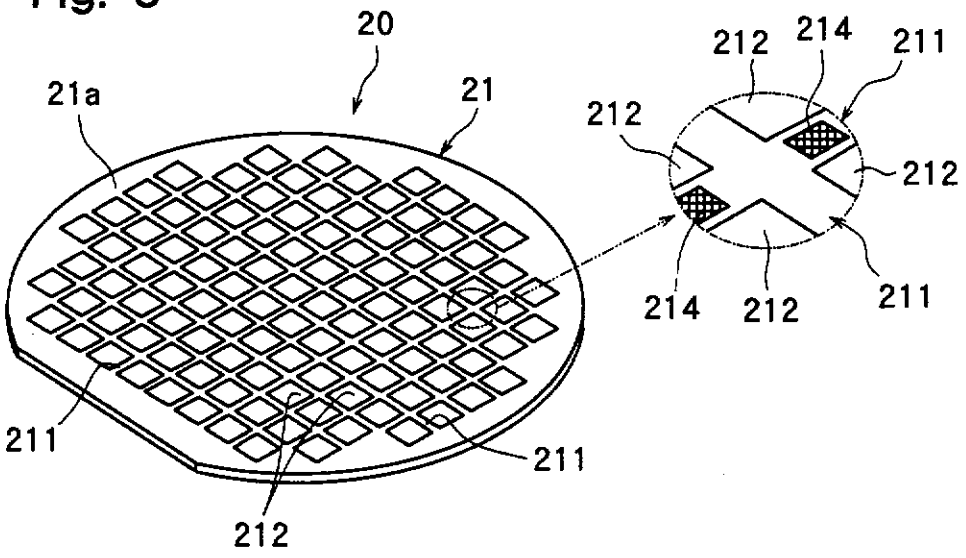


Fig. 4

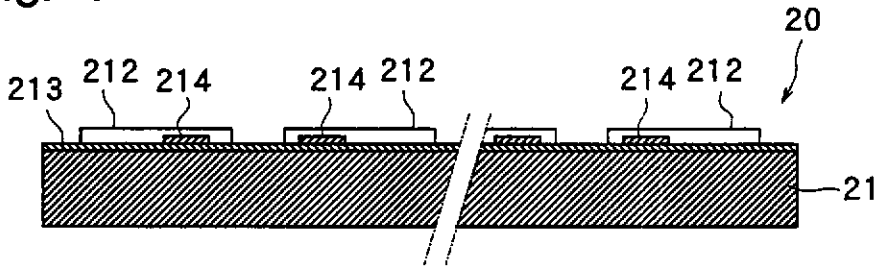
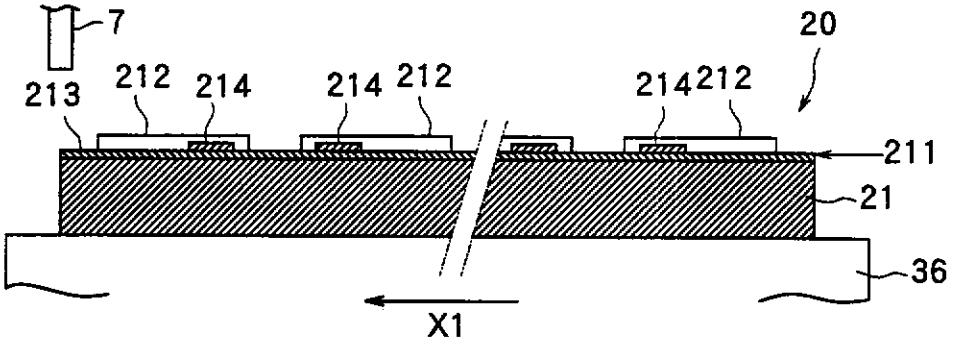


Fig. 5

(a)


7
213
212
214
214
212
214
212
20
211
21
36
X1

(b)

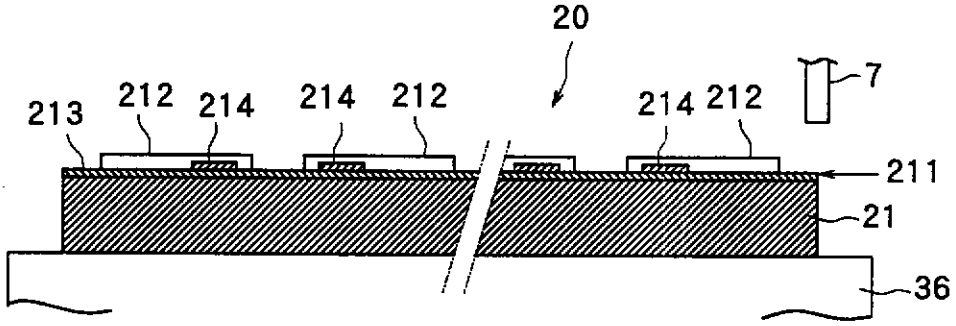
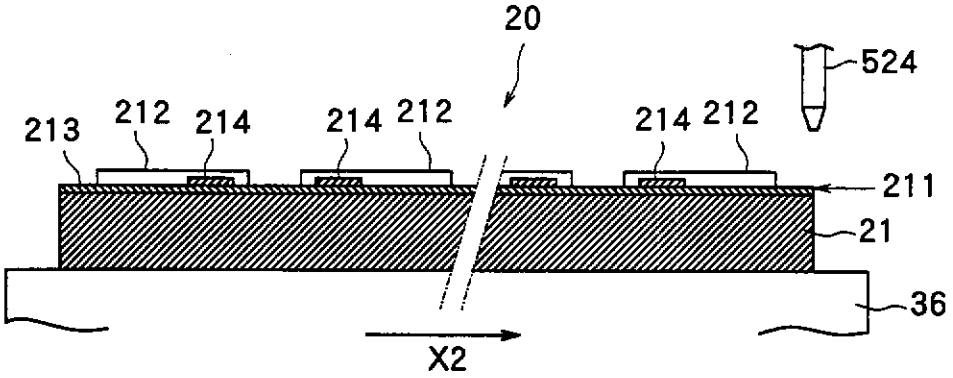

213
212
214
214
212
20
214
212
7
211
21
36

Fig. 6

(a)


20
524
213
212
214
214
212
214
212
211
21
36
X2

(b)

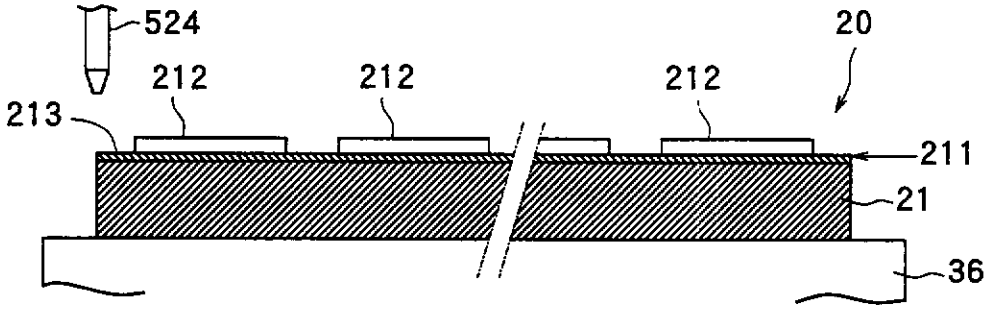
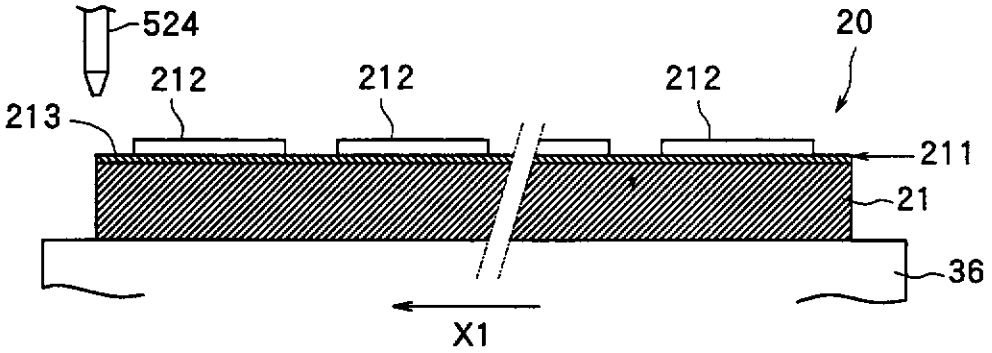

524
20
212
212
212
213
211
21
36

Fig. 7

(a)



(b)

