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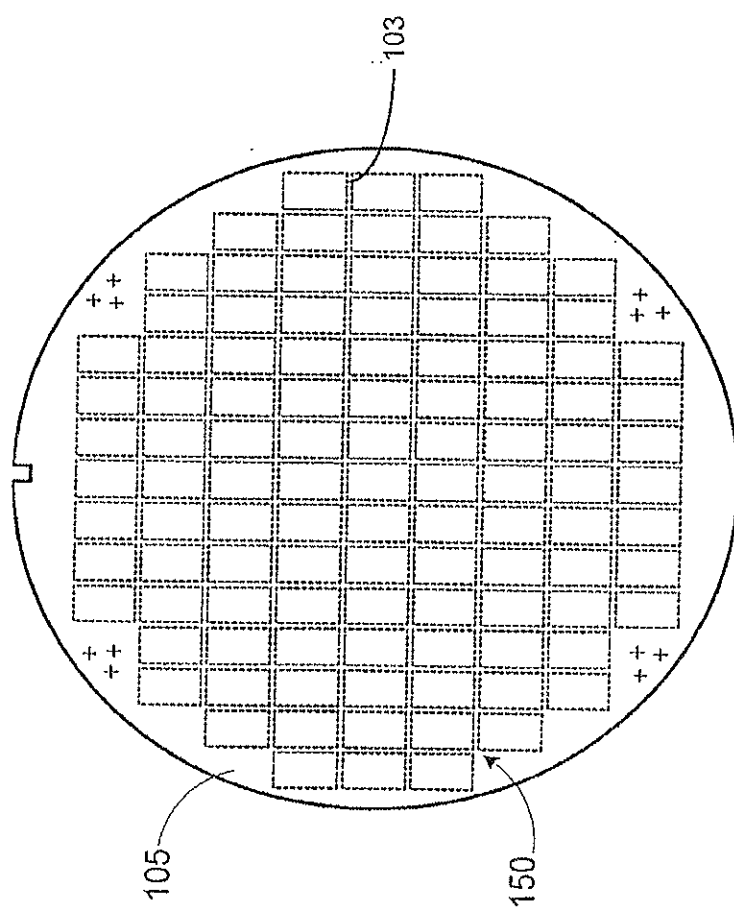


FIGURE 1 (Prior Art)

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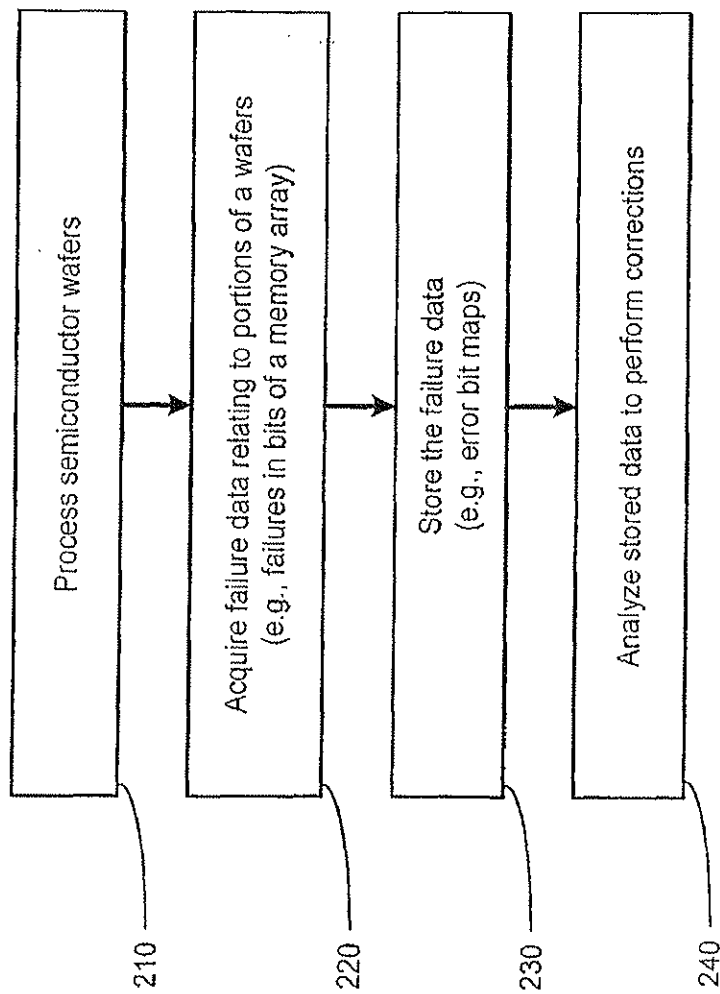


FIGURE 2 (Prior Art)

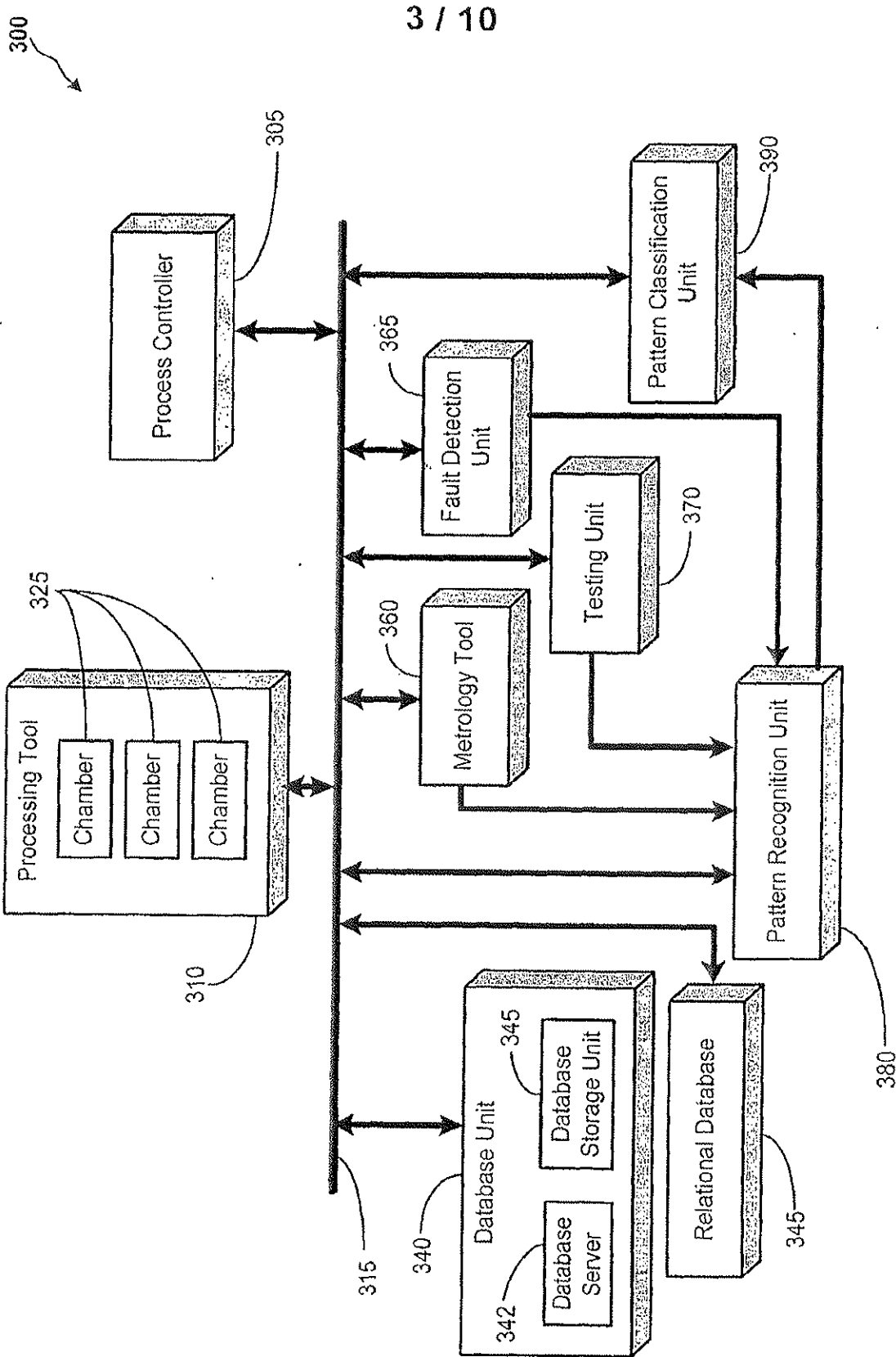


FIGURE 3

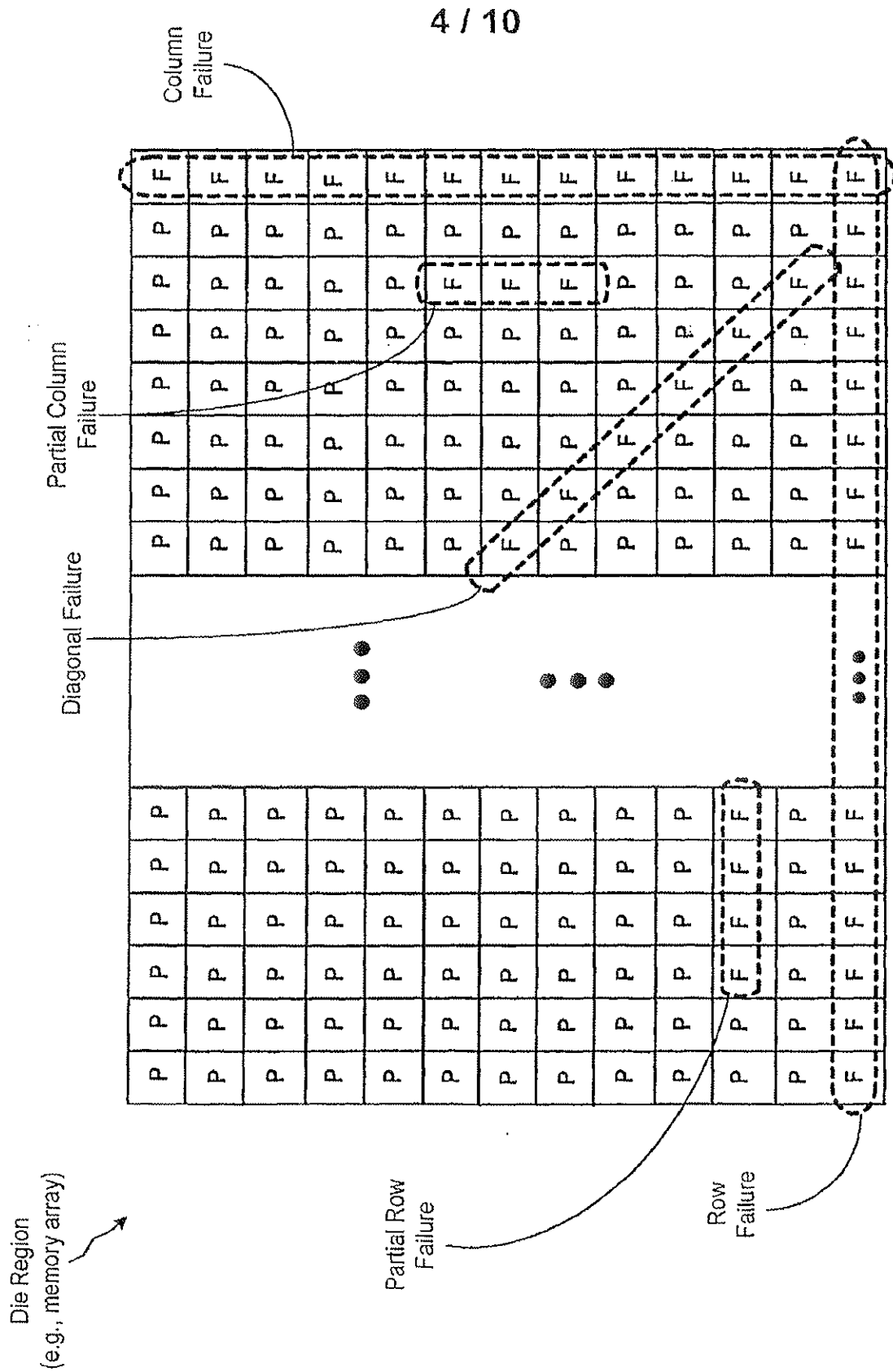
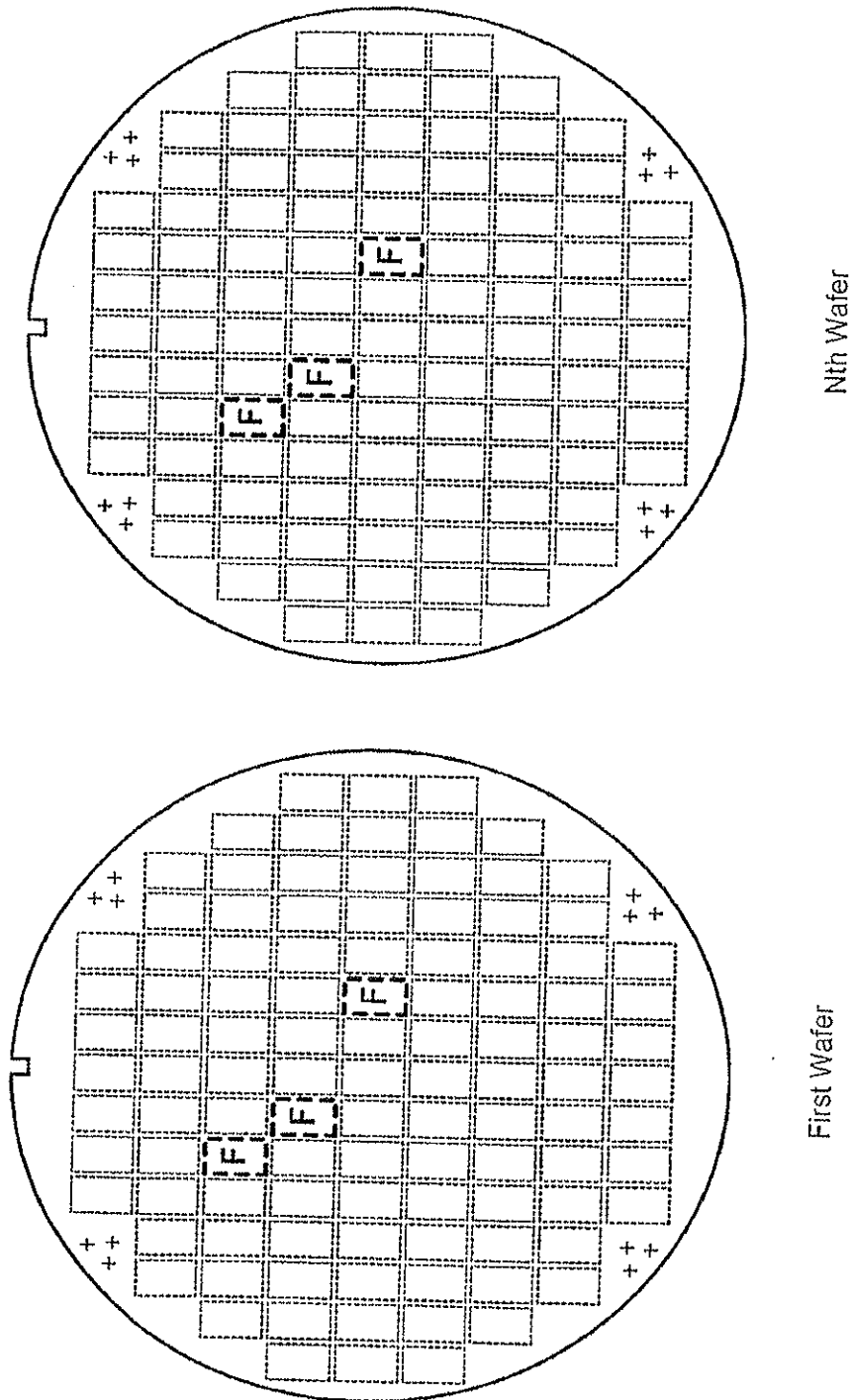


FIGURE 4

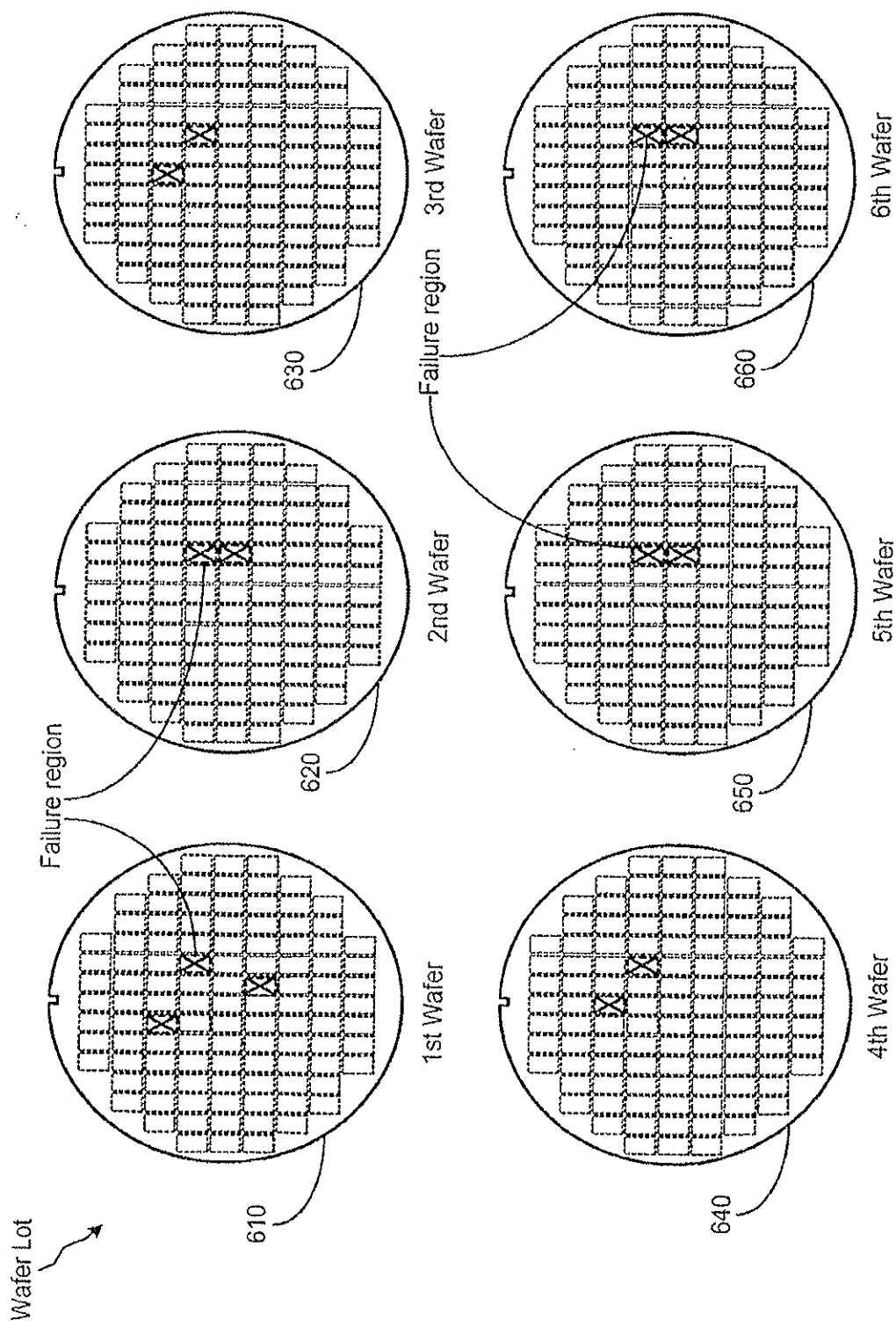
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Wafer-level Failure Pattern

FIGURE 5

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Lot-level Failure Patterns

FIGURE 6

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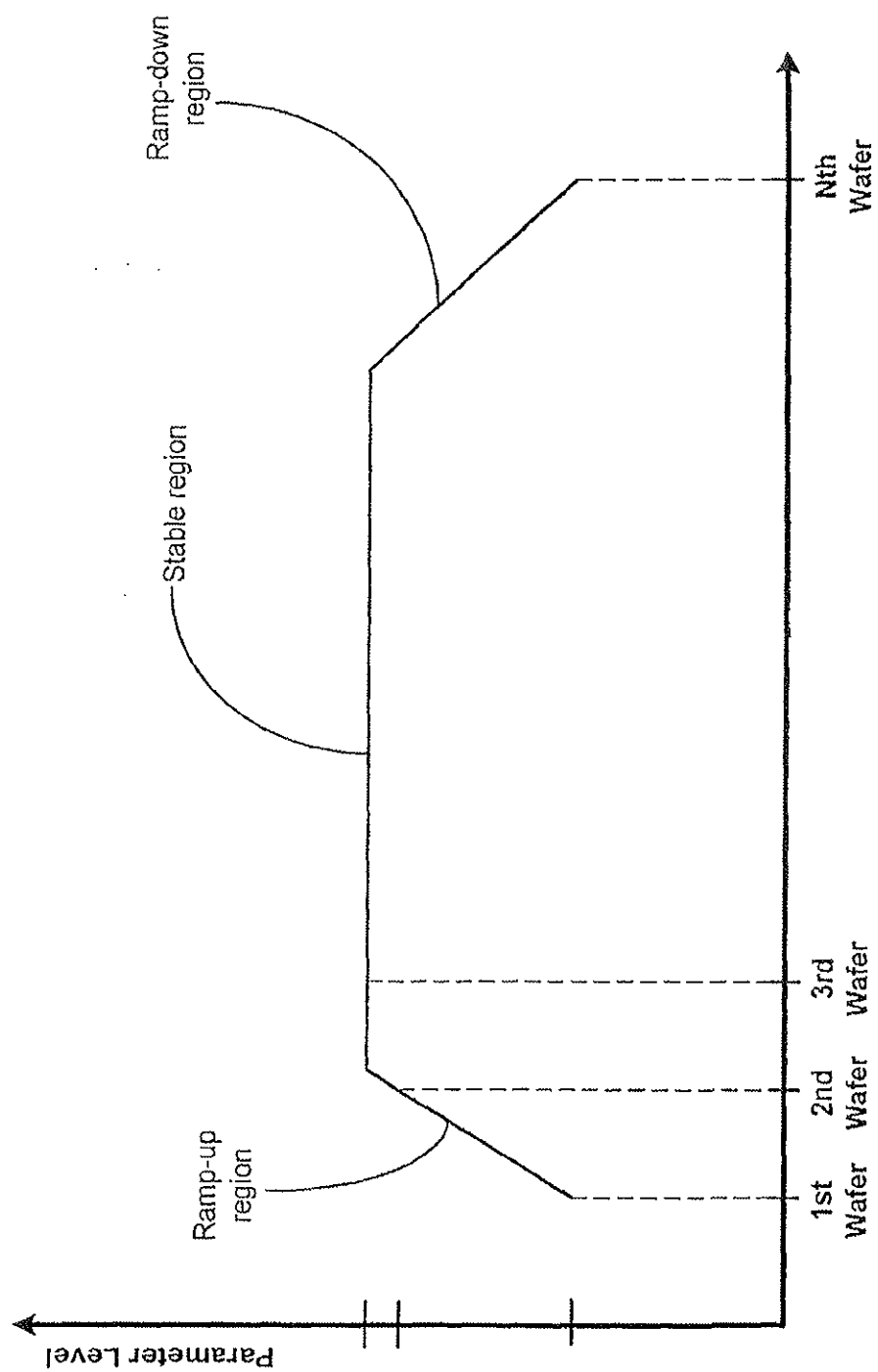


FIGURE 7A

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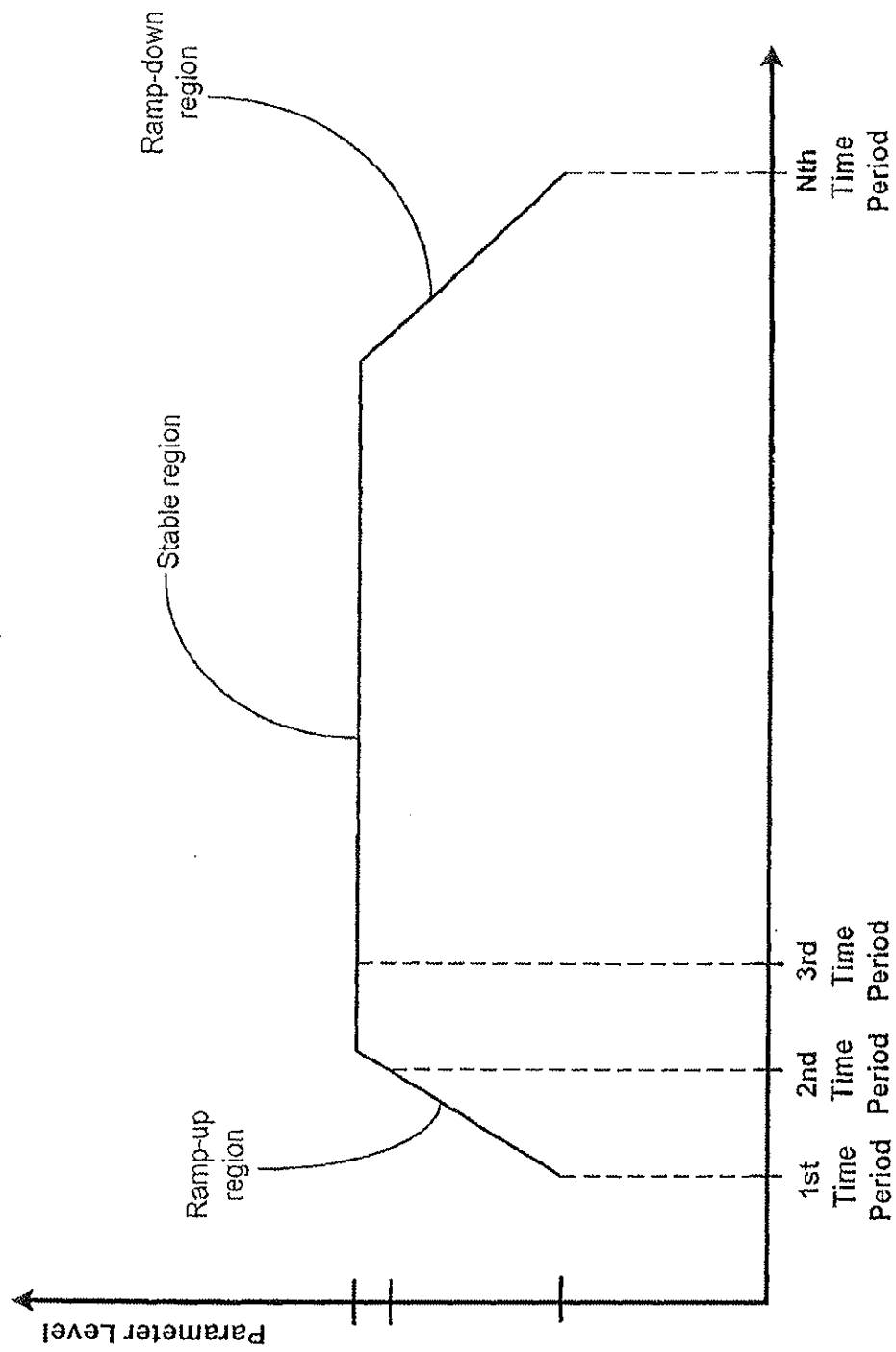


FIGURE 7B

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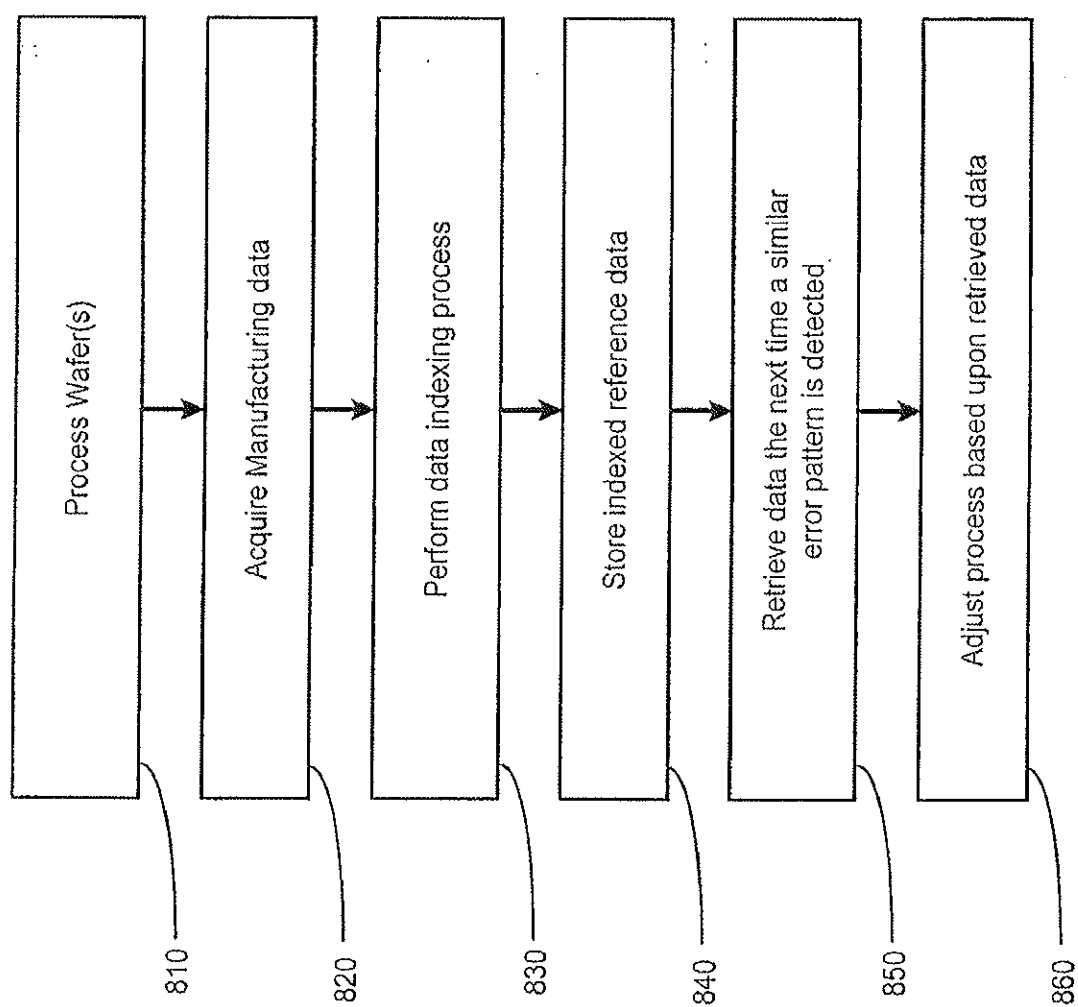


FIGURE 8

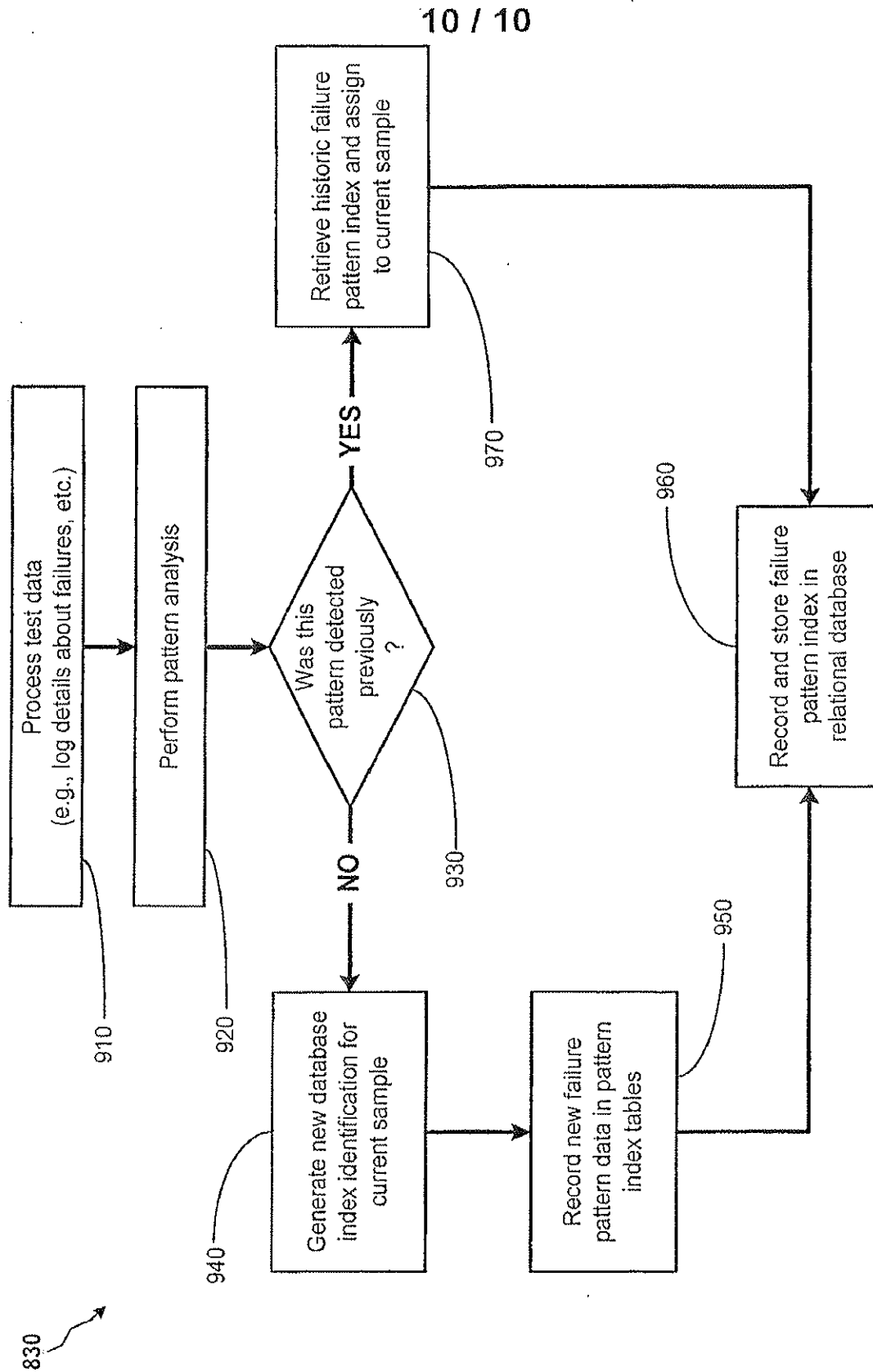


FIGURE 9