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IPDS

DISPLAY DRIVER SYSTEM AND METHOD FOR DRIVING DISPLAYS

FIELD OF THE INVENTION

This invention relates to a display driver system for controlling a display and a method for driving such a display. The invention is particularly useful for, but not necessarily limited to, a display driver and method for controlling a Liquid Crystal Display (LCD) used in a portable electronic device such as a portable communication device.

BACKGROUND ART

Portable communication devices, such as pagers, mobile (cellular) telephones and Personal Digital Assistants, all have a requirement to consume as little power as possible since they are battery operated and it is desirable to maintain a usable battery charge for as long as possible before replacement or recharging. Many communication devices typically include a LCD having one portion which is used to display alphanumeric (or other) characters on a dot matrix display comprising an array of addressable pixels to provide information to a user. Another portion of the LCD can used to display symbols, such as icons, which indicate the status of the device or other simple information.

The antenna of a portable communication device is generally sensitive to external noise and internal noise due to stray high frequency electromagnetic fields

emitted by components of the device. These undesirable frequencies mainly come from the clock source which is the highest fundamental frequency generated by any component of the device. Generally, the fundamental clock frequency can result in higher amplitude harmonics within the same receiving band. Thus, it is desirable to keep the fundamental frequency of the clock source as low as possible clock to thereby reduce internal noise.

To obtain a grey scale display, or colour display the control of the Root Mean Square Voltage (Vrms) is applied to the addressed pixels. As will be apparent to a person skilled in the art, Frame Rate Control (FRC) and Pulse Waveform Modulation (PWM) LCD driving system can be used to obtain grey scales or colour control. The FRC driving system that is commonly used in the large screen application and it is a high frequency driving. Such a high frequency driving is not recommended to portable communication devices due to the effects of internally generated noise.

There are three types of commonly used PWM driving systems known as leading edge PWM, lagging edge PWM and lead-lag PWM. However, the switching frequency for lead-lag PWM for a one of the drivers is half that of the leading or lagging edge PWM. However, conventional lead-lag PWM driving systems do may still require unnecessary amounts of power consumption to drive an LCD which can result in unacceptable or undesirable battery drain.

SUMMARY OF THE INVENTION

It is an aim of the invention to overcome or alleviate at least one of the problems associated with prior art PWM driving of displays.

According to one aspect of the invention there is provided a display driver system comprising:

a scan driver coupled to decoding circuitry, said scan driver having a plurality of parallel scan outputs for driving a display, said scan driver being adapted to cyclically provide pulses offset from each other on different said scan outputs, wherein at least some of said pulses adjacent in the time domain overlap; and

a pulse width modulation driver coupled to decoding circuitry, said pulse width modulation driver having a plurality of parallel modulation outputs for driving said display, said pulse width modulation driver being adapted to cyclically provide pulse width modulated signals on said modulation outputs, and at least some of said pulse width modulated signals adjacent in the time domain are modulated by at least part of a common signal.

Preferably, said display driver system may be further characterised by said at least some pulse width modulated signals adjacent in the time domain being modulated by lead-lag pulse width modulation. In another form, lag-lead pulse width modulation may be used.

Suitably, said display driver system may be operatively coupled to said display.

Preferably, said display may be a liquid crystal display. The display may be a monochrome or colour display.

Suitably, said scan driver may be adapted to toggle the polarity of said scan outputs at the completion of a cycle.

Preferably, said pulse width modulation driver may be adapted to toggle the polarity of said modulation outputs at the completion of a cycle.

Preferably, said scan driver and said pulse width modulation driver may be coupled to operate as a master slave relationship to effect toggling of their respective polarities.

Suitably, said decoding circuitry of said pulse width modulation driver may be coupled to a pulse width modulation signal generator. The pulse width modulation signal generator may have an input coupled to an output clock of a counter.

Preferably, said decoding circuitry of said scan driver may have an input coupled to an output clock of a counter.

According to another aspect of the invention there is method of driving a display:

cyclically generating scan pulses offset from each other on different parallel scan outputs of a scan driver, wherein at least some of said scan pulses that are adjacent in the time domain overlap;

cyclically generating pulse width modulated signals on modulation outputs of a pulse width modulation driver, whereby at least some of said pulse width modulated signals adjacent in the time domain are modulated by at least part of a common signal; and

supplying said scan pulses and said lead-lag pulse width modulated signals to a display to thereby selectively address individual elements thereof.

Preferably, the method may be further characterised by said at least some pulse width modulated signals adjacent in the time domain being modulated by lead-lag pulse width modulation. In another form, lag-lead pulse width modulation may be used.

Suitably, the method may be further characterised by the root mean square voltage at said individual elements is dependent upon at least one of said scan pulses and at least one of said lead-lag pulse width modulated signals, wherein said root mean square voltage on each of said elements affects the grey scale thereof.

Suitably, the method may be further characterised by the root mean square voltage at said individual elements is dependent upon at least one of said scan pulses and at least one of said lead-lag pulse width modulated signals, wherein said root mean square voltage on each of said elements affects the colour thereof.

Suitably, the method may be further characterised by said display being a liquid crystal display.

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the invention may be readily understood and put into practical effect, reference will now be made to a preferred embodiment as illustrated with reference to the accompanying drawings in which:

FIG. 1 shows a functional block diagram of a display driver system according to one embodiment of the invention;

FIG. 2 is a waveform at the output of a row decoder of the display driver system of FIG.1;

FIG. 3 is a waveform at the output of a row driver of the display driver system of FIG.1;

FIG. 4 is a pulse width modulation signal generator comprising part of the display driver system of FIG.1;

FIG. 5 is a waveform at the output of a column decoder of the display driver system of FIG.1;

FIG. 6 is a waveform at the output of a column driver of the display driver system of FIG.1; and

FIG. 7 is a waveform at a pixel of a LCD which is effectively a subtraction between output of a row driver and a column driver of the display driver system of FIG.1.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

Referring to FIG. 1, there is illustrated a display driver system 1 comprising a scan driver in the form of a row driver 2 and a pulse width modulation driver in the form of a column driver 3 having respective output buses 4,5 coupled to a display in the form of a LCD 6. Output bus 4 comprises n bits in for addressing rows of the LCD and output bus 5 comprises m bits for addressing m columns of the LCD 6.

There is also a power source 7 coupled to provide a voltage to row and column drivers 2,3. Typically power source 7 provides a voltage of 7 Volts Direct Current

(DC) for a 32 bit column LCD. The row driver 2 is coupled to the column driver 3 by line 8 to thereby provide a polarity synchronisation signal so that both drivers 2,3 remain in the same polarity.

The display driver system 1 also includes a row decoder 9 having an output bus 21 of n bits coupled to row driver 2 and a strobe output STROBE coupled to an input of an OR gate 10, the output of which is coupled to an enable input of row driver 2. A clock input Ck of row decoder 9 is coupled to an output out1 of a counter 11 which in use supplies a clock signal of frequency f1. An output out2 of counter 11 is coupled to a pulse width modulation signal generator (PWMSG) 12 which in use supplies a clock frequency f2.

The driver system 1 also includes a PWM column decoder 13 having inputs coupled to outputs of PWMSG 12 by a 16 bit timing bus 14. Outputs of PWM column decoder 13 are coupled to inputs of column driver 3 by a bus 15 and an enable input of PWM column decoder 3 is coupled via an OR gate 16 to PWMSG 12. A display data Random Access Memory 17 has an output bus 22 of m bits coupled to PWM column decoder 13 and an enable input of display data Random Access Memory 17 is coupled to an output of an OR gate 18.

A microprocessor unit 19 has an output data bus coupled to display data Random Access Memory 17 and a clock output Ck coupled clock inputs of counter 11 and a clock input of a Random Access Memory decoder module 20. The microprocessor unit 19 also has an enable output EN coupled to enable inputs of row decoder 9, PWMSG 12, OR gates 10, 16, 18 and Random Access Memory decoder module 20. Further, the Random Access Memory decoder module 20 has an output coupled to an input of OR gate 18.

In use, the microprocessor unit 19 initially provides an enable pulse to synchronise the display driver system 1. The clock output of the microprocessor unit 19 also provides a base clock for synchronising the display driver system 1. In this regard, the pulse counter 11 supplies clock frequencies f1 and f2, which are dependent upon the frequency of the base clock from microprocessor unit 19. Clock frequency f1 is supplied to row decoder 9 which in turn provides an output signal on bus 21 as illustrated in FIG. 2 which correspond to n bits of output bus 4. This signal comprises a cyclic scan pulse on each of the n bits of bus 21, each pulse adjacent in the time domain overlaps by a period t1 and typically each refresh cycle is 16 milli seconds. As will be apparent to a person skilled in the art, row decoder 9 provides a strobe signal to clock the signal on bus 21 to row driver 2.

In Fig. 3 there is illustrated the waveforms at output 4 from row driver 2. As shown there is toggling of the outputs on each n bits after each a refresh cycle. The waveforms at output 4 are related to the cyclic scan pulses on bus 21 and such toggling is known in the art and is effected within row driver 2 by use of power supplied from power source 7.

In Fig. 4 there is illustrated an embodiment of PWMSG 12 which comprises a16 grey level PWM output signals T1 to T16 on timing bus 14. The PWMSG 12 comprises 18 synchronously coupled D type flip flops forming a 16 bit shift register which are supplied with clock frequency f2 from counter 11.

In Fig. 5 the output signals T1 to T16 on bus 14 are illustrated in which synchronised pulses on each bus line vary in width and are synchronised with the rest of driving system 1 to thereby provide a lead-lag sequence

of pulses supplied to column decoder 13. The display data Random Access Memory 17 controlled by microprocessor unit 19 , decoder 20 and other logic provide a row of display data to column decoder 13 along bus 22.

Accordingly, output signals T1 to T16 and the row of display data are processed by column decoder 13 to provide data to column driver 3 along bus 15 in which at least part of each common signal (for example lead-lag pulses on T1) pulse width modulates the output of some of the signals adjacent in time at the output bus 15 of column decoder 13. As a result, output 5 will supply waveforms to LCD 6 as illustrated in Fig. 6, these waveforms being lead-lag pulse width modulated. As shown, there is a toggling of the outputs on each m bits after each a refresh cycle. The waveforms at output 5 are related to the cyclic scan pulses on bus 15. The toggling is synchronised to the polarity of row driver 2 by a master slave relationship communicated along line 8 and is effected within row driver 3 by use of power supplied from power source 7.

The waveforms applied at outputs 4,5 result in a selectable driving signal being applied on each pixel of the LCD 6 as illustrated in Fig. 7. This resultant signal applied to each pixel determines the grey level (or colour) for that specific pixel which is effectively a subtraction between an output of row driver 2 and column driver 3. The grey level is dependent upon the RMS value applied to the specific pixel over a 16 millisecond period (due to the refresh cycle in this embodiment being 16 milli seconds).

The present invention allows for driving a display by cyclically generating scan pulses offset from each other on different parallel scan outputs of a the scan driver system 1. Some of the scan pulses at the

output of row driver 2 that are adjacent in the time domain are generated to overlap. The driver system 1 also cyclically generates pulse width modulated signals on modulation outputs of column driver 3, whereby at least some of the pulse width modulated signals adjacent in the time domain are modulated by at least part of a common signal (T1 to T16). The driver system 1 supplies the scan pulses and the lead-lag pulse width modulated signals to the LCD 6 to thereby selectively address individual elements thereof.

Advantageously, the present invention does not require a clock frequency as high as that used with conventional display driver systems. This is because the cyclic scan pulse on each of the n bits of bus 21 overlap an adjacent scan pulse in the time domain by a period t1 which therefore allows for increased widths of the scanning pulses within a refresh cycle. Further, the driving voltage can be reduced and reduced switching due to the use of lead-lag PWM also increases battery life.

Although the invention has been described with reference to a preferred embodiment, it is to be understood that the invention is not restricted the embodiment described herein.



WE CLAIM:

1. A display driver system comprising:

a scan driver coupled to decoding circuitry, said scan driver having a plurality of parallel scan outputs for driving a display, said scan driver being adapted to cyclically provide pulses offset from each other on different said scan outputs, wherein at least some of said pulses adjacent in the time domain overlap; and

a pulse width modulation driver coupled to decoding circuitry, said pulse width modulation driver having a plurality of parallel modulation outputs for driving said display, said pulse width modulation driver being adapted to cyclically provide pulse width modulated signals on said modulation outputs, and at least some of said pulse width modulated signals adjacent in the time domain are modulated by at least part of a common signal.

2. A display driver system as claimed in claim 1, wherein said at least some pulse width modulated signals adjacent in the time domain are modulated by lead-lag pulse width modulation.

3. A display driver system as claimed in any one preceding claim, wherein said display driver system is operatively coupled to said display.

4. A display driver system as claimed in any one preceding claim, wherein said display is a liquid crystal display.

5. A display driver system as claimed in any one preceding claim, wherein said scan driver is adapted to toggle the polarity of said scan outputs at the completion of a cycle.

* C L M S *

toggle the polarity of said scan outputs at the completion of a cycle.

6. A display driver system as claimed in any one preceding claim, wherein said pulse width modulation driver is adapted to toggle the polarity of said modulation outputs at the completion of a cycle.

7. A display driver system as claimed in any one preceding claim, wherein said scan driver and said pulse width modulation driver are coupled to operate as a master slave relationship to effect toggling of their respective polarities.

8. A display driver system as claimed in any one preceding claim, wherein said decoding circuitry of said pulse width modulation driver is coupled to a pulse width modulation signal generator.

9. A method of driving a display comprising the steps of:

cyclically generating scan pulses offset from each other on different parallel scan outputs of a scan driver, wherein at least some of said scan pulses that are adjacent in the time domain overlap;

cyclically generating pulse width modulated signals on modulation outputs of a pulse width modulation driver, whereby at least some of said pulse width modulated signals adjacent in the time domain are modulated by at least part of a common signal; and

supplying said scan pulses and said lead-lag pulse width modulated signals to a display to thereby selectively address individual elements thereof.

10. A method of driving a display as claimed in claim 9, wherein said at least some pulse width modulated signals adjacent in the time domain being modulated by lead-lag pulse width modulation.

11. A method of driving a display as claimed in claim 9 or claim 10, wherein the root mean square voltage at said individual elements is dependent upon at least one of said scan pulses and at least one of said pulse width modulated signals, and

wherein said root mean square voltage on each of said elements affects the grey scale thereof.

12. A method of driving a display as claimed in any one of claims 9 to 11, wherein the root mean square voltage at said individual elements is dependent upon at least one of said scan pulses and at least one of said pulse width modulated signals,

wherein said root mean square voltage on each of said elements affects the colour thereof.

13. A method of driving a display as claimed in any one of claims 9 to 12, wherein said display is a liquid crystal display.

14. A display driver system as described herein with reference to and as illustrated by the accompanying illustrations.

15. A method of driving a display substantially as described herein with reference to and as illustrated by the accompanying illustrations.

This Sheet Has Been Replaced

THIS SHEET HAS BEEN REPLACED

DISPLAY DRIVER SYSTEM AND METHOD FOR DRIVING DISPLAYS

ABSTRACT OF THE DISCLOSURE

A display driver system (1) having a scan driver (2) coupled to decoding circuitry (9), the scan driver has a plurality of parallel scan outputs (4) for driving a Liquid Crystal Display (6), The scan driver (2) cyclically provides pulses offset from each other on different scan outputs (4), wherein at least some of these pulses adjacent in the time domain overlap. The display driver system (1) has a pulse width modulation driver (3) coupled to decoding circuitry (13), the pulse width modulation driver (3) has a plurality of parallel modulation outputs (5) for driving the Liquid Crystal Display (6). The pulse width modulation driver (3) is adapted to cyclically provide pulse width modulated signals on the modulation outputs (5), and at least some of the pulse width modulated signals adjacent in the time domain are modulated by at least part of a common signal.

Figure 1 accompanies this abstract.

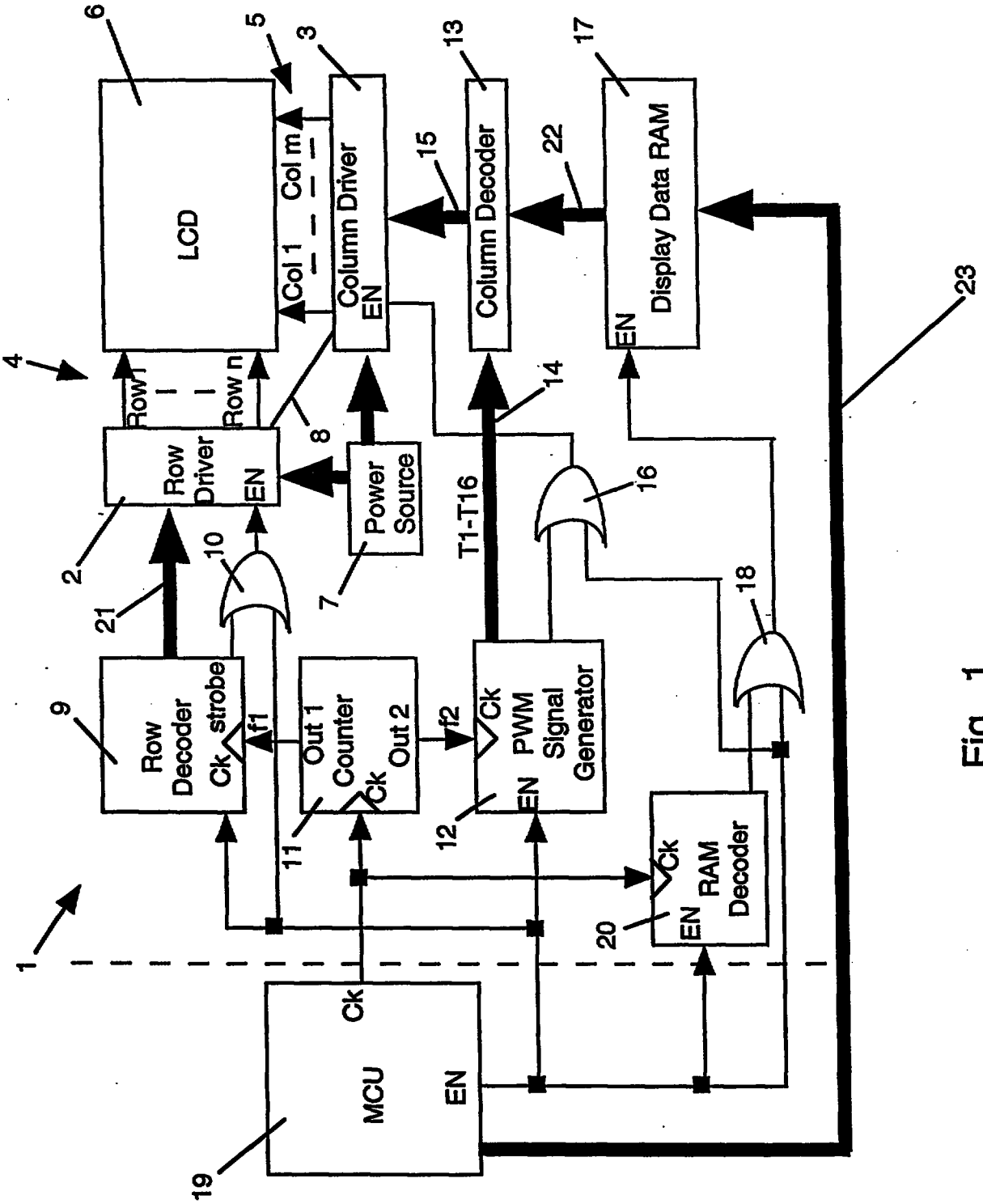

LCD
Col 1
Col m
Column Driver
EN
Column Decoder
Display Data RAM
EN
Row 1
Row n
Row Driver
EN
Power Source
T1-T16
Row Decoder
Ck
strobe
f1
Out 1 Counter
Ck
Out 2
f2
Ck
PWM Signal Generator
EN
Ck
RAM Decoder
EN
Ck
MCU
EN
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23

Fig. 1

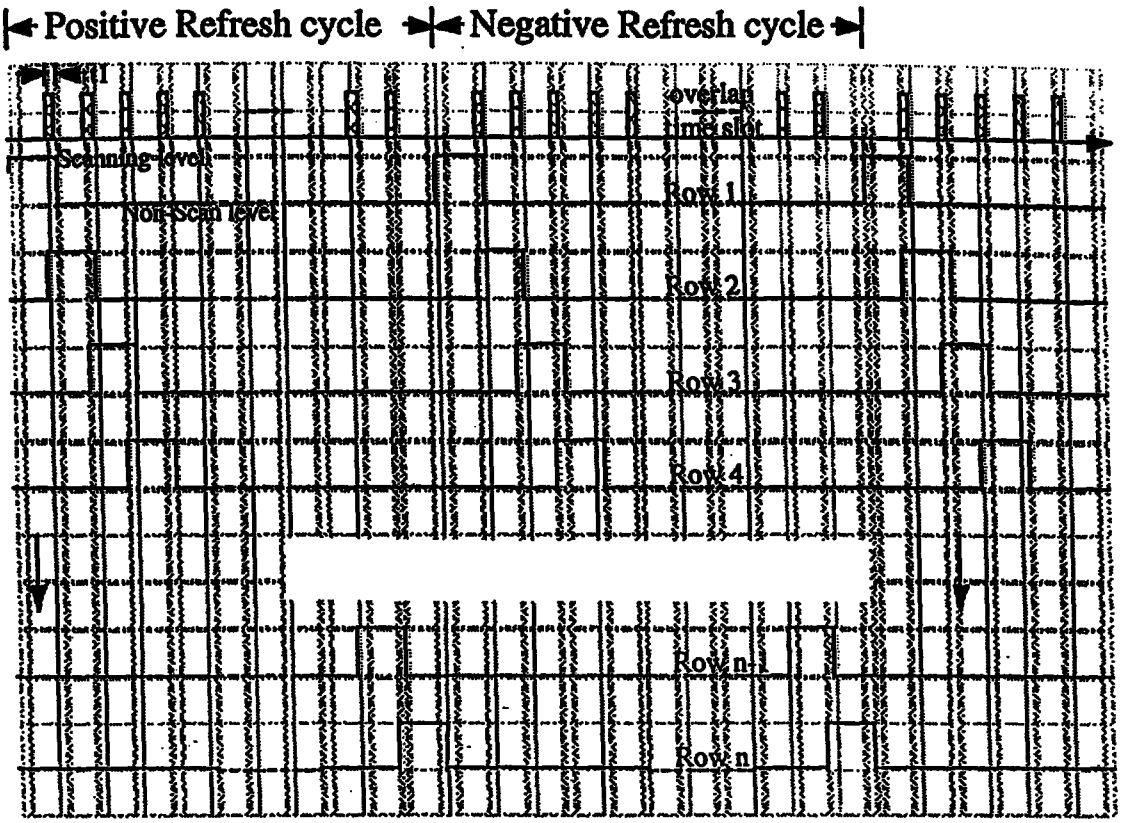

Positive Refresh cycle
Negative Refresh cycle
overlap time slot
Scanning level
Non-Scan level
Row 1
Row 2
Row 3
Row 4
Row n-1
Row n

FIG. 2

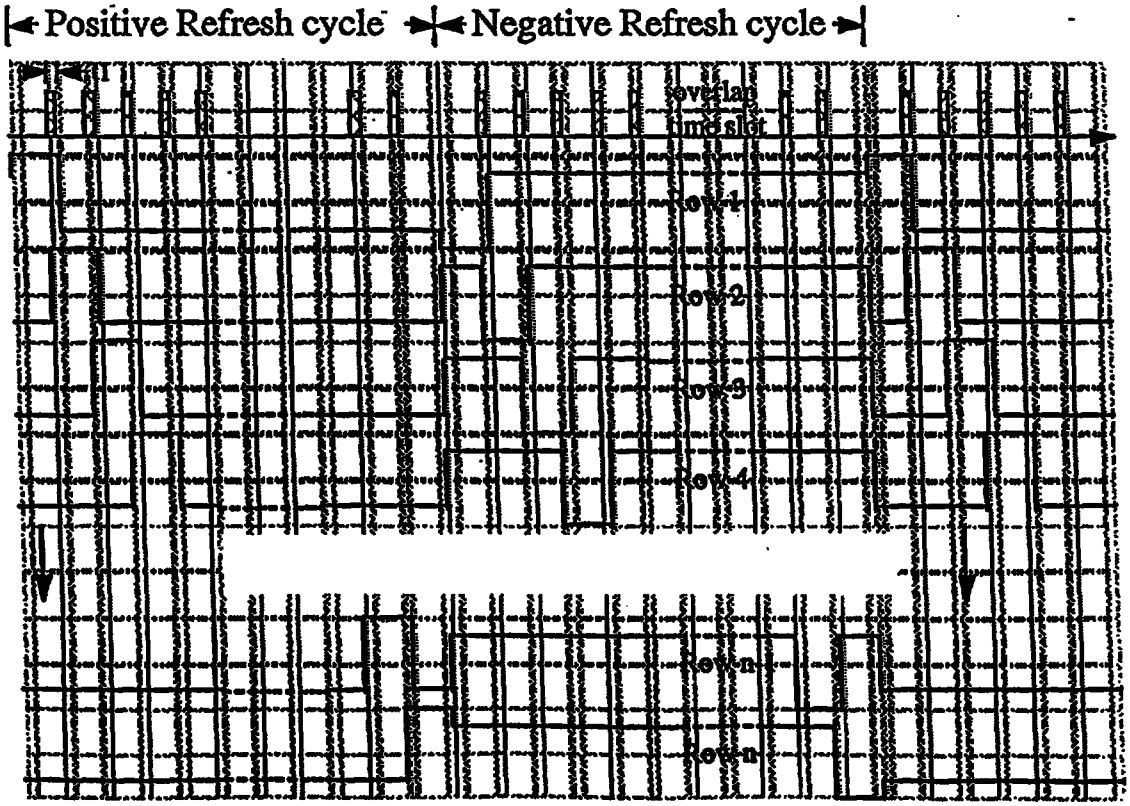

Positive Refresh cycle
Negative Refresh cycle
overlap time slot
Row 1
Row 2
Row 3
Row 4
Row n
Row n

FIG. 3

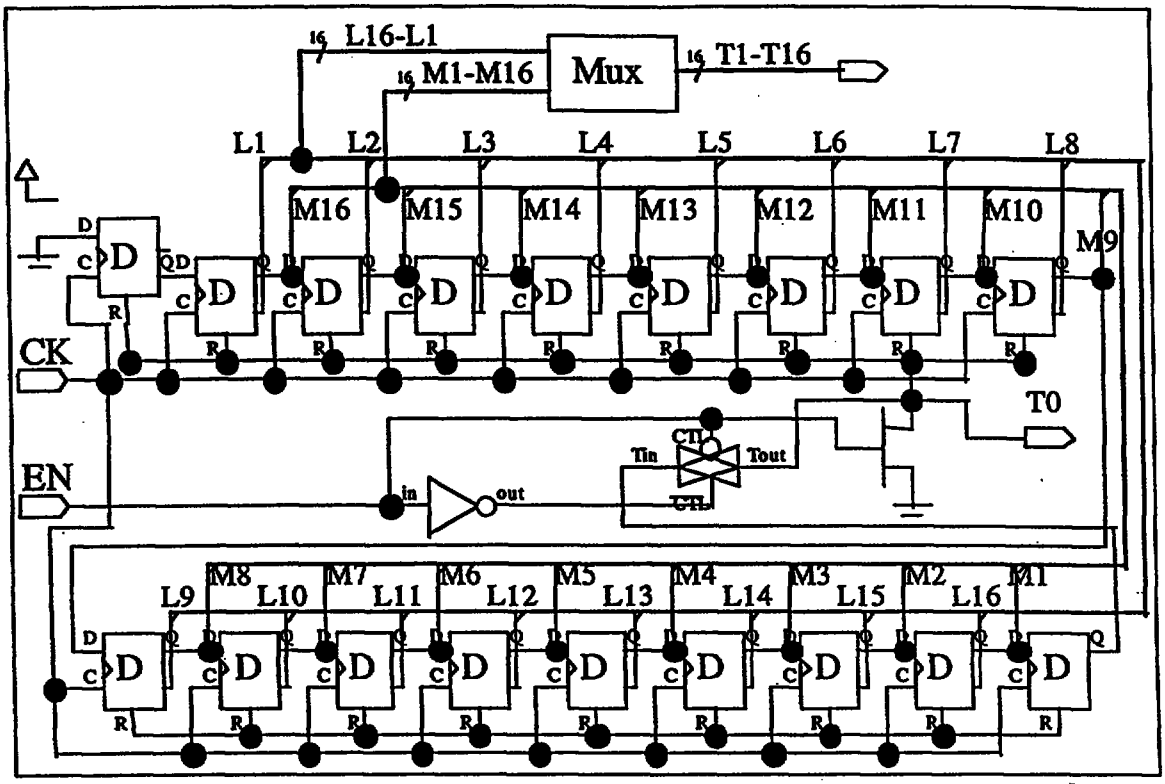

16 L16-L1
16 M1-M16
Mux
16 T1-T16
L1
L2
L3
L4
L5
L6
L7
L8
M16
M15
M14
M13
M12
M11
M10
M9
CK
EN
T0
Tin
Tout
in
out
M8
M7
M6
M5
M4
M3
M2
M1
L9
L10
L11
L12
L13
L14
L15
L16

FIG. 4

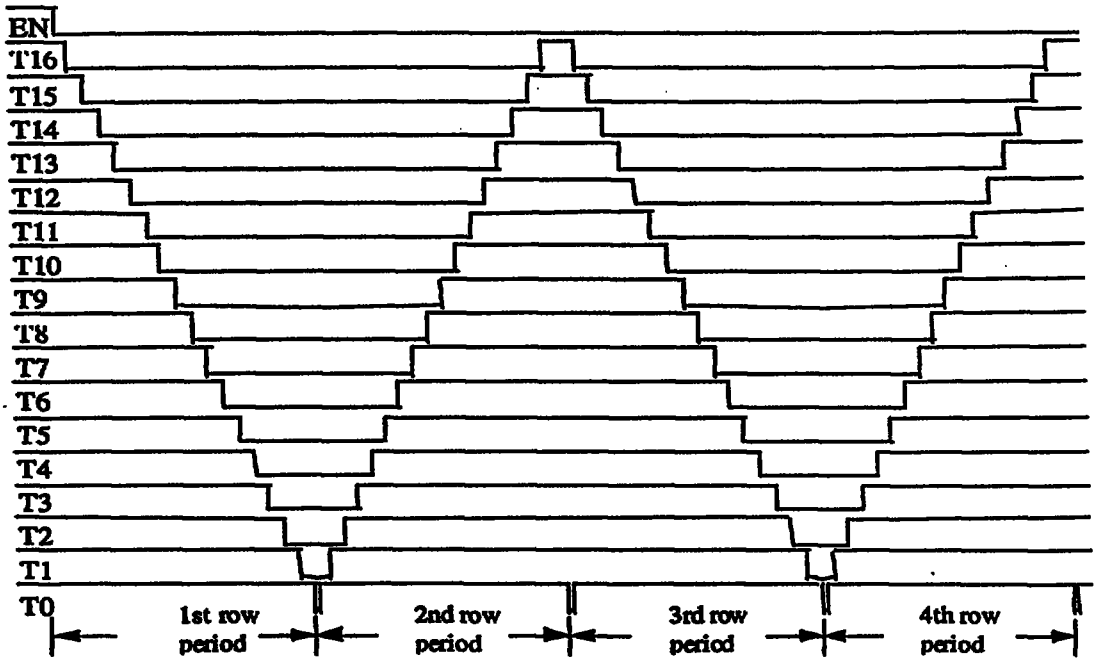

EN
T16
T15
T14
T13
T12
T11
T10
T9
T8
T7
T6
T5
T4
T3
T2
T1
T0
1st row period
2nd row period
3rd row period
4th row period

FIG. 5

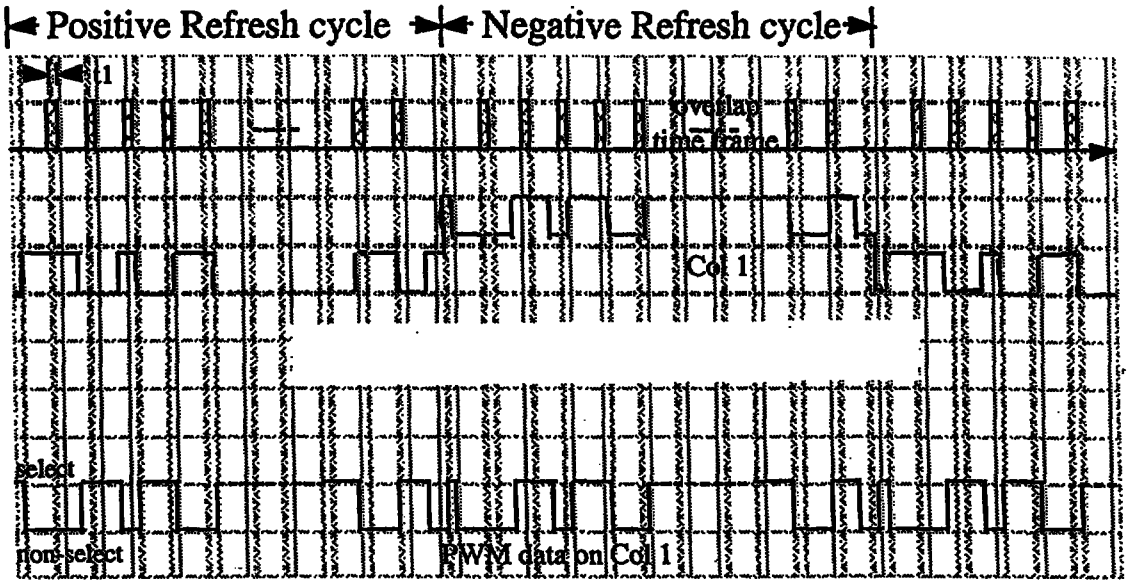


FIG. 6

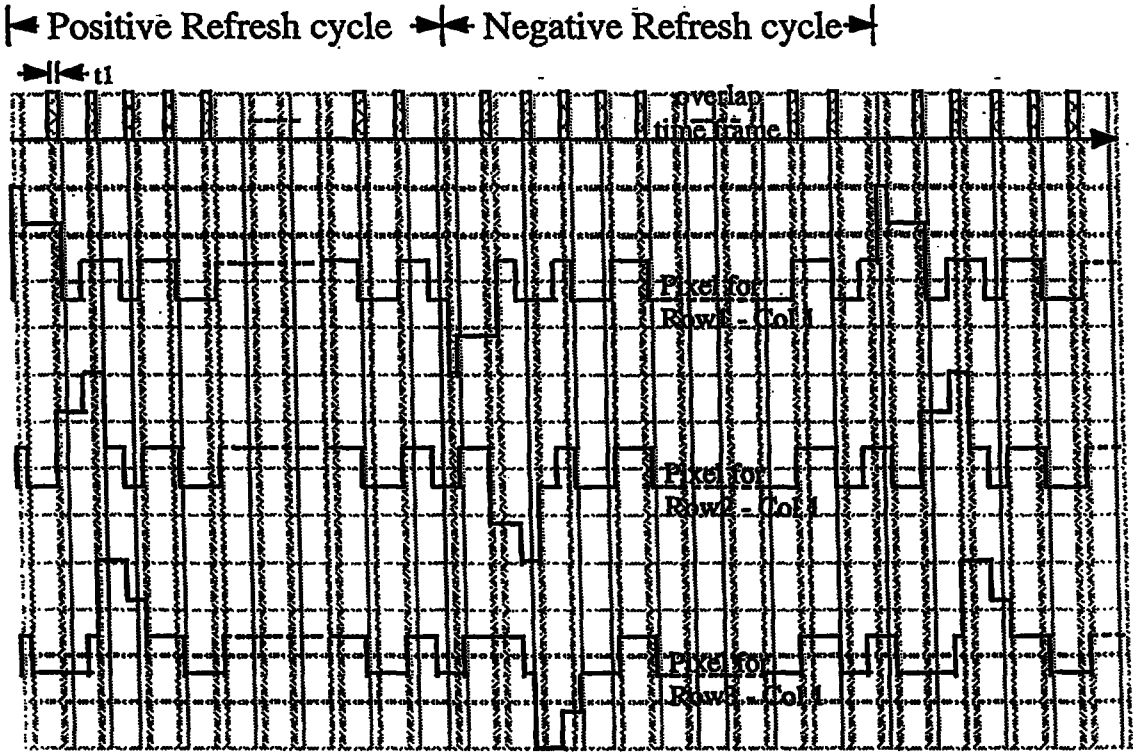


Figure 7

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10. A method of driving a display as claimed in claim 9, wherein said at least some pulse width modulated signals adjacent in the time domain being modulated by lead-lag pulse width modulation.

11. A method of driving a display as claimed in claim 9 or claim 10, wherein the root mean square voltage at said individual elements is dependent upon at least one of said scan pulses and at least one of said pulse width modulated signals, and

wherein said root mean square voltage on each of said elements affects the grey scale thereof.

12. A method of driving a display as claimed in any one of claims 9 to 11, wherein the root mean square voltage at said individual elements is dependent upon at least one of said scan pulses and at least one of said pulse width modulated signals,

wherein said root mean square voltage on each of said elements affects the colour thereof.

13. A method of driving a display as claimed in any one of claims 9 to 12, wherein said display is a liquid crystal display.

REPLACEMENT SHEET
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