(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 April 2002 (11.04.2002)

PCT

(10) International Publication Number
WO 02/029557 A3

(51) International Patent Classification[7]: G06F 9/38, 9/455

(21) International Application Number: PCT/US01/42533

(22) International Filing Date: 5 October 2001 (05.10.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/684,113 6 October 2000 (06.10.2000) US

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(81) Designated States *(national)*: CN, JP, KR, SG.

Published:
— *with international search report*

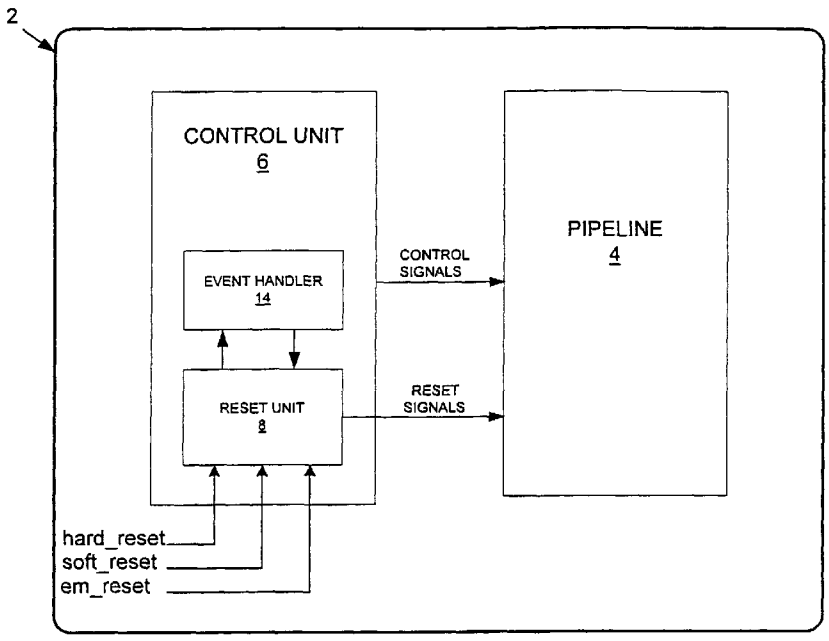
(88) Date of publication of the international search report:
15 August 2002

(48) Date of publication of this corrected version:
13 February 2003

(15) Information about Correction:
see PCT Gazette No. 07/2003 of 13 February 2003, Section II

[Continued on next page]

(54) Title: RESETTING A PROGRAMMABLE PROCESSOR



(57) Abstract: In one embodiment, a pipelined processor includes a reset unit that provides an output reset signal to at least one stage of the pipeline. The reset unit is adapted to detect at least a hard reset request, a soft reset request and an emulation reset request. The pipeline comprises N stages and the reset unit asserts the reset signal for at least N cycles of a clock after the reset request has been cleared. Each stage if the pipeline has a storage circuit for storing a corresponding valid bit. At least one of the storage circuits is cleared in response to the reset signal. In addition, the reset unit handles the reset request as a reset event having an assigned priority.

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