

WHAT IS CLAIMED IS:

1. A vertical-type memory device, comprising:
 - a substrate having a cell array region and a connection region adjacent to the cell array region;
 - a plurality of gate electrode layers stacked on the cell array region and the connection region of the substrate, the plurality of gate electrode layers forming a stepped structure in the connection region;
 - a cell channel layer in the cell array region, the cell channel layer passing through the plurality of gate electrode layers;
 - at least one dummy channel layer in the connection region, the at least one dummy channel layer passing through at least one gate electrode layer of the plurality of gate electrode layers;
 - a cell epitaxial layer disposed below the cell channel layer; and
 - at least one dummy epitaxial layer disposed below the at least one dummy channel layer,wherein the at least one dummy epitaxial layer has a shape that is different from a shape of the cell epitaxial layer, and
 - wherein the at least one dummy channel layer is electrically insulated from the substrate by an insulating material.
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2. The vertical-type memory device as claimed in claim 1, wherein the at least one dummy epitaxial layer has an upper region and a lower region having different shapes.

3. The vertical-type memory device as claimed in claim 2, further comprising insulating layers disposed on a side wall of a portion of the at least one dummy epitaxial layer and extending to the at least one dummy channel layer,

wherein the upper region and the lower region of the at least one dummy epitaxial layer are separated from each other by the insulating layers.

4. The vertical-type memory device as claimed in claim 2 or claim 3, wherein:
the cell epitaxial layer is in contact with the cell channel layer, and
the lower region of the at least one dummy epitaxial layer is spaced apart from the at least one dummy channel layer.

5. The vertical-type memory device as claimed in any one of claims 2 to 4, wherein the upper region of the at least one dummy epitaxial layer has a ring shape.

6. The vertical-type memory device as claimed in claim 5, wherein a thickness of the upper region of the at least one dummy epitaxial layer changes in a direction away from a center thereof.

7. The vertical-type memory device as claimed in any one of claims 2 to 6, wherein an upper surface of the lower region of the at least one dummy epitaxial layer includes a ring-shaped protrusion portion.

8. The vertical-type memory device as claimed in claim 7, wherein the protrusion portion has a pointed end portion.

9. The vertical-type memory device as claimed in claim 3, wherein the at least one dummy epitaxial layer is separated from the at least one dummy channel layer by the insulating layers.

10. The vertical-type memory device as claimed in any one of claims 1 to 9, wherein an upper surface of the at least one dummy epitaxial layer includes a ring-shaped protrusion portion.

11. The vertical-type memory device as claimed in claim 10, wherein the protrusion portion has a pointed end portion.

12. The vertical-type memory device as claimed in any one of claims 1 to 11, wherein:

the at least one dummy channel layer includes a plurality of dummy channel layers,
the at least one dummy epitaxial layer includes a plurality of dummy epitaxial layers, and

heights of the plurality of dummy epitaxial layers are reduced in a direction from a portion of the connection region adjacent to the cell array region toward an outer edge of the connection region.

13. The vertical-type memory device as claimed in claim 12, further comprising:

a plurality of gate dielectric layers surrounding the plurality of dummy channel layers; and

a plurality of voids disposed below the plurality of gate dielectric layers, respectively, in the connection region.

14. The vertical-type memory device as claimed in claim 13, wherein positions of the voids of the plurality of voids move closer to the substrate in a direction from a portion of the connection region adjacent to the cell array region toward the outer edge of the connection region.

15. A vertical-type memory device, comprising:

a substrate having a cell array region and a connection region located outside the cell array region;

a plurality of gate electrode layers stacked on the cell array region and the connection region of the substrate, the plurality of gate electrode layers forming a stepped structure in the connection region;

a dummy channel layer disposed in the connection region, the dummy channel layer passing through the plurality of gate electrode layers; and

a dummy epitaxial layer disposed below the dummy channel layer,

wherein the dummy epitaxial layer includes an upper region and a lower region spaced apart from each other with an insulating material therebetween.

16. The vertical-type memory device as claimed in claim 15, further comprising a void between the upper region and the lower region, the void being sealed by the insulating material.

17. The vertical-type memory device as claimed in claim 15 or claim 16, wherein:

the upper region has a ring shape, and

a thickness of the upper region changes in a direction away from a center thereof.

18. A vertical-type memory device, comprising:

a substrate;

a plurality of gate electrode layers stacked on the substrate;

a dummy channel hole passing through at least one among the plurality of gate electrode layers;

a gate dielectric layer in the dummy channel hole;

an upper dummy epitaxial layer in contact with a lower surface of the gate dielectric layer; and

a lower dummy epitaxial layer spaced apart from the upper dummy epitaxial layer with an insulating material therebetween.

19. The vertical-type memory device as claimed in claim 18, wherein the upper dummy epitaxial layer and the lower dummy epitaxial layer have different shapes.

20. The vertical-type memory device as claimed in claim 18 or claim 19, further comprising a dummy channel layer on the gate dielectric layer,

wherein the dummy channel layer is electrically insulated from the lower dummy epitaxial layer.