Semiconductor Constructions and Transistors, and Methods of Forming Semiconductor Constructions and Transistors

TECHNICAL FIELD

[0001] The invention pertains to methods of forming semiconductor constructions such as memory circuitry, and more particularly, to forming memory cells, DRAMs, and transistors.

BACKGROUND OF THE INVENTION

[0002] As integrated circuitry continues to shrink in size, efforts are ongoing to find novel methods of forming integrated circuitry structures and related integrated circuitry which improve upon those methods currently utilized and the resultant structures formed thereby. One type of integrated circuitry is memory circuitry and arrays. Such circuitry has been and continues to be the focus of intense efforts to reduce the size of the circuitry, increase the speed with which such circuitry operates, and maintain or increase the ability of such circuitry to perform its memory function. The industry designers continually search for ways to reduce the size of memory circuitry without sacrificing array performance.

[0003] One such way is by improving on the design of transistor structures which are incorporated into memory circuitry. Transistor structures or devices have numerous applications for semiconductor circuitry. For instance, transistor structures can be incorporated into memory circuitry (such as, for example, dynamic random access memory (DRAM)) and logic circuitry. DRAM circuitry usually includes an array of memory cells interconnected by rows and columns, which are known as word lines and

digit lines (or bit lines), respectively. A typical DRAM memory cell comprises a transistor structure connected with a charge storage device or data storage element (such as, for example, a capacitor device).

[0004] Typical transistor structures comprise a channel region between a pair of source/drain regions, and a gate configured to electrically connect the source/drain regions to one another through the channel region. The transistor constructions utilized in semiconductor constructions will be supported by a semiconductor substrate. The semiconductor substrate will have a primary surface which can be considered to define a horizontal direction or horizontal surface. Transistor devices can be divided amongst two broad categories based upon the orientations of the channel regions relative to the primary surface of the semiconductor substrate. Specifically, transistor structures which have channel regions that are primarily parallel to the primary surface of the substrate are referred to as planar transistor structures, and those having channel regions which are generally perpendicular to the primary surface of the substrate are referred to as vertical transistor structures. Since current flow between the source and drain regions of a transistor device occurs through the channel region, planar transistor devices can be distinguished from vertical transistor devices based upon the direction of current flow as well as on the general orientation of the channel region. Specifically, vertical transistor devices are devices in which the current flow between the source and drain regions of the devices is primarily substantially orthogonal to a primary surface of a semiconductor substrate, and planar transistor devices are devices in which the current flow between source and drain regions is primarily parallel to the primary surface of the semiconductor substrate.

[0005] There is a continuing interest in the development of methodologies by which vertical transistor devices can be incorporated into integrated circuitry applications due to, among other things, advantages in packing density that can be obtained utilizing vertical transistor devices relative to planar transistor devices. Difficulties are frequently encountered in attempting to produce the vast arrays of vertical transistor devices desired for semiconductor applications while maintaining suitable performance characteristics of the devices. For example, present methodologies for forming vertical transistor devices include forming or growing epitaxial silicon posts or pillars to extend upward from the primary or horizontal surface of the semiconductor substrate. The epitaxial silicon posts or pillars are used as the transistor channels in present designs of vertical transistor devices. However, this design creates several problems. For example, a high defect density has resulted with potential cell leakage issues. Additionally, the design promotes a floating body effect in the transistor channel which complicates and increases the difficulty of controlling the gate threshold voltage of the transistor. Accordingly, it is desired to develop new methods for fabricating vertical transistor devices that improve upon and/or at least diminish or alleviate these problems.

SUMMARY OF THE INVENTION

[0006] In one aspect, the invention encompasses a transistor device that includes a semiconductor substrate. The device also includes a gate formed to extend within the semiconductor substrate, a gate dielectric formed over the gate, a pair of source/drain

regions formed on opposite sides of the gate, and a channel region formed within the semiconductor substrate.

[0007] In another aspect, the invention encompasses a transistor device that includes a semiconductor substrate that has an upper surface. A pair of source/drain regions are formed within the semiconductor substrate. A channel region is formed within the semiconductor substrate and extends generally perpendicularly relative to the upper surface of the semiconductor substrate. A gate is formed between the pair of the source/drain regions.

[0008] In still another aspect, the invention encompasses a semiconductor construction that includes a conductive post extending upward from an upper surface of a semiconductor substrate. A source/drain region is formed below the conductive post within the semiconductor substrate and is electrically coupled with the conductive post. A transistor channel extends below the source/drain and a gate is formed within the semiconductor substrate adjacent the transistor channel.

[0009] In yet another aspect, the invention encompasses a method of forming a semiconductor construction that includes providing a semiconductor substrate with an opening. An oxide film is formed over the semiconductor substrate within the opening. A conductive gate material is provided over the oxide film and fills the opening. A pair of diffusion regions is formed on opposite sides of the gate material within the semiconductor substrate and a channel region is defined to extend generally vertically within the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0011] Fig. 1 is a diagrammatic, top plan fragmentary view of a semiconductor construction at a preliminary processing stage of an exemplary aspect of the present invention.

[0012] Fig. 2 is a cross-sectional view taken along line 2-2 of the Fig. 1 fragment.

[0013] Fig. 3 is a view of the Fig. 1 fragment shown at a processing stage subsequent to that of Fig. 1.

[0014] Fig. 4 is a cross-sectional view taken along line 4-4 of the Fig. 3 fragment.

[0015] Fig. 5 is a view of the Fig. 3 fragment shown at a processing stage subsequent to that of Fig. 3.

[0016] Fig. 6 is a cross-sectional view taken along line 6-6 of the Fig. 5 fragment.

[0017] Fig. 7 is a view of the Fig. 5 fragment rotated 90 degrees.

[0018] Fig. 8 is a cross-sectional view taken along line 8-8 of the Fig. 7 fragment.

[0019] Fig. 9 is a view of the Fig. 5 fragment shown at a processing stage subsequent to that of Fig. 5.

[0020] Fig. 10 is a cross-sectional view taken along line 10-10 of the Fig. 9 fragment.

[0021] Fig. 11 is a view of the Fig. 9 fragment rotated 90 degrees.

[0022] Fig. 12 is a cross-sectional view taken along line 12-12 of the Fig. 11 fragment.

[0023] Fig. 13 is a view of the Fig. 9 fragment shown at a processing stage subsequent to that of Fig. 9.

[0024] Fig. 14 is a cross-sectional view taken along line 14-14 of the Fig. 13 fragment.

[0025] Fig. 15 is a view of the Fig. 13 fragment rotated 90 degrees.

[0026] Fig. 16 is a cross-sectional view taken along line 16-16 of the Fig. 15 fragment.

[0027] Fig. 17 is a view of the Fig. 13 fragment shown at a processing stage subsequent to that of Fig. 13.

[0028] Fig. 18 is a cross-sectional view taken along line 18-18 of the Fig. 17 fragment.

[0029] Fig. 19 is a view of the Fig. 17 fragment rotated 90 degrees.

[0030] Fig. 20 is a cross-sectional view taken along line 20-20 of the Fig. 19 fragment.

[0031] Fig. 21 is a view of the Fig. 17 fragment shown at a processing stage subsequent to that of Fig. 17.

[0032] Fig. 22 is a cross-sectional view taken along line 22-22 of the Fig. 21 fragment.

[0033] Fig. 23 is a view of the Fig. 21 fragment rotated 90 degrees.

[0034] Fig. 24 is a cross-sectional view taken along line 24-24 of the Fig. 23 fragment.

[0035] Fig. 25 is a view of the Fig. 21 fragment shown at a processing stage subsequent to that of Fig. 21.

[0036] Fig. 26 is a cross-sectional view taken along line 26-26 of the Fig. 25 fragment.

[0037] Fig. 27 is a view of the Fig. 25 fragment rotated 90 degrees.

[0038] Fig. 28 is a cross-sectional view taken along line 28-28 of the Fig. 27 fragment.

[0039] Fig. 29 is a view of the Fig. 25 fragment shown at a processing stage subsequent to that of Fig. 25.

[0040] Fig. 30 is a cross-sectional view taken along line 30-30 of the Fig. 29 fragment.

[0041] Fig. 31 is a view of the Fig. 29 fragment rotated 90 degrees.

[0042] Fig. 32 is a cross-sectional view taken along line 32-32 of the Fig. 31 fragment.

[0043] Fig. 33 is a view of the Fig. 29 fragment shown at a processing stage subsequent to that of Fig. 29.

[0044] Fig. 34 is a cross-sectional view taken along line 34-34 of the Fig. 33 fragment.

[0045] Fig. 35 is a view of the Fig. 33 fragment rotated 90 degrees.

[0046] Fig. 36 is a cross-sectional view taken along line 36-36 of the Fig. 35 fragment.

[0047] Fig. 37 is a view of the Fig. 33 fragment shown at a processing stage subsequent to that of Fig. 33.

[0048] Fig. 38 is a cross-sectional view taken along line 38-38 of the Fig. 37 fragment.

[0049] Fig. 39 is a view of the Fig. 37 fragment rotated 90 degrees.

[0050] Fig. 40 is a cross-sectional view taken along line 40-40 of the Fig. 39 fragment.

[0051] Fig. 41 is a view of the Fig. 37 fragment shown at a processing stage subsequent to that of Fig. 37.

[0052] Fig. 42 is a cross-sectional view taken along line 42-42 of the Fig. 41 fragment.

[0053] Fig. 43 is a view of the Fig. 41 fragment rotated 90 degrees.

[0054] Fig. 44 is a cross-sectional view taken along line 44-44 of the Fig. 43 fragment.

[0055] Fig. 45 is a view of the Fig. 41 fragment shown at a processing stage subsequent to that of Fig. 41.

[0056] Fig. 46 is a cross-sectional view taken along line 46-46 of the Fig. 45 fragment.

[0057] Fig. 47 is a view of the Fig. 45 fragment rotated 90 degrees.

[0058] Fig. 48 is a cross-sectional view taken along line 48-48 of the Fig. 47 fragment.

[0059] Fig. 49 is a cross-sectional fragmentary view of a semiconductor construction at a final processing stage of one exemplary embodiment of the present invention at a processing stage subsequent to that of Figs. 45-48.

[0060] Fig. 50 is a view of the Fig. 49 fragment rotated 90 degrees.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0061] This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

[0062] With respect to memory integrated circuitry, the area over a substrate required for each memory cell in a memory array partially determines the capacity of the device. This area is a function of the number of elements in each memory cell and the size of each of the elements. For conventional memory cells, the area is stated to be $8F^2$, where F represents a minimum feature size for photolithographically-defined features and the dimensions of the conventional cell area is 2F by 4F. These memory cell dimensions and areas are readily understood by referring to U.S. Patent Application Publication No. 2003/0234414 A1, published December 25, 2003, the disclosure of which is incorporated herein by reference. U.S. Patent Application Publication No. 2003/0234414 A1 discloses state-of-the-art memory devices wherein the memory cells have cell areas on the order of $4F^2$. By review of the U.S. Patent Application Publication No. 2003/0234414 and comparing such disclosure to the disclosure of the present invention, it should be understood that, the present invention discloses memory circuitry that includes memory cell areas on the order of $4F^2$.

[0063] Now referring to Figs. 1 and 2 (Fig. 2 a cross section of Fig. 1), a semiconductor construction 10 comprises a substrate 12 having a primary surface 13 oriented generally horizontally and is alternatively described as an upper surface. Substrate 12 can comprise, consist essentially of, or consist of a monocrystalline semiconductor material, and in particular aspects will comprise, consist essentially of, or

consist of monocrystalline silicon lightly-doped with appropriate background-type dopant. For example, substrate 12 can be a portion of a monocrystalline silicon wafer. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. In one exemplary embodiment, substrate 12 comprises a bulk semiconductor substrate or bulk wafer, for example, a monocrystalline silicon substrate or wafer.

[0064] Still referring to Figs. 1-2, isolation regions 14 are formed in substrate 12. In one exemplary embodiment, isolation regions 14 comprise shallow trench isolation (STI) regions. The isolation regions 14 extend generally in parallel and spaced rows leaving regions 16 of substrate 12 between respective rows of isolation regions 14. Regions 16 of substrate 12 are defined by isolation regions 14 and are configured as parallel and spaced rows having upper surfaces 13.

[0065] Referring to Figs. 3 and 4, (Fig. 4 is a cross section of Fig. 3), a nitride layer 18 is deposited over upper surface 13 of substrate 12 and isolations regions 14. An exemplary thickness of nitride layer 18, that is the height in which nitride layer 18 extends upward from upper surface 13, ranges from about 2,000 Angstroms to about 3,000 Angstroms.

[0066] Referring to Figs. 5-8, it should be understood that all four figures represent the same processing step. Figs. 5-6 represent a first orientation and Figs. 7-8 represent a second orientation that is oriented 90 degrees from the orientation of Figs. 5-6. Nitride layer 18 is patterned and etched to form trenches 20 (Fig. 8) that extend down to substrate 12 to expose upper surface portions 22 of substrate 12. Trenches 20 also expose isolation region portions 24 of isolation regions 14. The nitride layer 18 is left patterned as nitride rows or runners 18 that extend generally in a spaced and parallel relation oriented perpendicularly to the direction of the isolation regions 14. Upper surface portions 22 of substrate 12 are generally bounded by isolation region portions 24 of isolation regions 14 and nitride rows 18, and are generally shaped as squares. In one exemplary embodiment, the etching step includes an over-etch of substrate to range from 0 to about 300 angstroms.

[0067] Referring to Figs. 9-12, isolation region portions 24 are etched to recess isolation regions 14 elevationally below upper surface portions 22 of substrate 12 leaving recessed surfaces 26 of isolation regions 14 (Fig. 10). In one exemplary embodiment, the etch process comprises a Reactive Ion Etch (R.I.E.) and would be selective to the nitride runners 18 and exposed silicon of substrate 12, for example, upper surface portions 22. The recess etch exposes sidewalls 27 of substrate 12 which were originally covered by the insulative material of isolation regions 14. The isolation regions 14 are recessed from a range of about 500 to about 1,500 angstroms below upper surface portions 22 with another exemplary recess range of about 800 to about 1,500 angstroms. In one exemplary embodiment, a recess distance between recessed surfaces 26 and upper surface portions 22 equals about 1,000 angstroms. A clean etch

is performed to remove residual oxide from over sidewalls 27 and upper surface portions 22 of substrate 12 with an exemplary clean etch being a wet hydrofluoric (HF) etch.

[0068] Referring to Figs. 13-16, a nitride liner 28 is provided over substrate 12 and structures formed thereon to protect exposed portions of isolation regions 14 (e.g., recessed surfaces 26 illustrated in Figs. 9-12). In one exemplary embodiment, a thickness for nitride liner 28 ranges from about 30 to about 100 angstroms. A sacrificial layer 30, for example, a spin-on-glass (SOG) layer is provided to fill trenches 20 between nitride runners 18. Other exemplary materials for sacrificial layer 30 includes borophosphorus silicate glass (BPSG) and/or a TEOS layer. A planar etch is performed to planarize the SOG layer 30 until the planar etch stops at nitride rows 18 wherein nitride rows 18 function as an etch stop. An exemplary planar etch comprises CMP (chemical mechanical polishing) processing.

[0069] Referring to Figs. 17-20, the SOG layer 30 is patterned and selectively etched to remove portions of SOG layer 30 to form openings 31 through the SOG layer 30 to expose nitride liner 28 over upper surface portions 22 of substrate 12. Exemplary configurations of exposed portions of nitride liner 28 are squares. Portions of SOG layer 30 remain as towers extending upward from substrate 12 between nitride runners 18 with exemplary configurations for the towers being rectangular. The exposed portions of the nitride liner 28 are removed to expose the upper surface portions 22 of substrate 12. An exemplary etch to remove the portions of nitride liner 28 from over upper surface portions 22 includes a selective nitride etch. After removal of the portions of nitride liner 28 from over upper surface portions 22, openings 31 extend to upper

surface portions 22 and are defined or bordered by the towers of SOG layer 30 and nitride rows 18. An exemplary selective nitride etch will over-etch nitride, for example nitride rows 18, from 0 to about 300 angstroms and preferably stop at silicon substrate 12. In one exemplary embodiment, the exposed upper surface portions 22 of substrate 12 define general surface areas of substrate 12 that will serve or function as active areas for subsequently formed devices and/or structures.

[0070] Referring to Figs. 21-24, a blanket insulative layer, for example a TEOS layer, is formed over silicon substrate 12 and fills openings 31. The exemplary TEOS layer is anisotropically etched to form sacrificial TEOS spacers 34 over nitride rows 18 and SOG layer 30. An exemplary etch includes a reactive ion etch leaving sacrificial TEOS spacers 34 laterally extending from about 200 to about 500 angstroms from the sides of nitride rows 18 and SOG layer 30. The sacrificial TEOS spacers 34 narrow openings 31 leaving generally cylindrical openings 32 exposing a smaller surface area of upper surface portions 22. In one exemplary embodiment, TEOS spacers 34 improve the critical dimensions possible for subsequently formed structures provide over or upon upper surface portions 22 of silicon substrate 12.

[0071] Referring to Figs. 25-28, in some but not all embodiments, a nitride material is provided over silicon substrate 12 to fill cylindrical openings 32 and then anisotropically etched to form another nitride liner 36 (the first nitride liner being 28) over sacrificial TEOS spacers 34. An exemplary anisotropic etch will provide a nitride liner 36 having a thickness ranging from about 50 to about 200 angstroms. After the anisotropically etch to form nitride liner 36, a reactive ion etch is performed to remove nitride liner 36 from over upper surface portions 22 of silicon substrate 12 wherein upper

surface portions 22 of silicon substrate 12 are again exposed. In one exemplary embodiment, the nitride liner 36 will protect TEOS spacers 34 during subsequent etch processing and/or during subsequent silicidation processing.

[0072] Referring to Figs. 29-32, in an exemplary embodiment, further etching and planarization processing can be performed to elevationally lower the upper surfaces of nitride rows 18 and SOG layer 30 relative silicon substrate 12 to a pre-selected elevation or height above upper surface portions 22. Such pre-selected height of nitride rows 18 and SOG layer 30 facilitates the formation of a pre-selected height of subsequently formed epitaxial structures relative substrate 12. Posts or pillars 38 are formed extending upward from exposed upper surface portions 22 of silicon substrate 12 through cylindrical openings 32. In one exemplary embodiment, posts or pillars 38 comprise epitaxial silicon grown or formed from exposed upper surfaces portions 22 of silicon substrate 12. Posts 38 have upper surfaces 39 and, in one exemplary embodiment, upper surfaces 39 are formed elevationally below upper surfaces 47 of nitride rows 18 with an exemplary elevational difference being about 1,000 to about 1,500 angstroms. Exemplary posts 38 comprise a height (measured from about upper surface portions 22 to upper surface 39) of about 1,000 to about 1,500 angstroms. Alternatively, an exemplary height of epitaxial silicon posts 38 can be considered in terms of a percentage height relationship relative the height of nitride rows 18 extending from silicon substrate 12. For example, epitaxial silicon posts 38 are formed to extend from upper surface portions 22 to be within about 50% to about 70% of the height of nitride rows 18, and a further exemplary range of about 60% to about 65% of the height of nitride rows 18. In some embodiments, epitaxial silicon posts 38 will serve or function

as an electrical contact between a charge storage device or data storage element (such as, for example, a capacitor device) and a transistor formed in subsequent processing, and explained more thoroughly below. Alternatively considered, posts 38 will serve or function as a node region, for example a source/drain region, discussed more thoroughly subsequently.

[0073] An exemplary alternative process to forming epitaxial silicon posts 38 is to deposit a conductive material over substrate 12 wherein cylindrical openings 32 are filled with the conductive material. In this alternative process, conductive material extending outward of cylindrical openings 32 is removed by exemplary planar or blanket etching, preferably down to upper surfaces 47 of nitride rows 18. The conductive material is then recessed into the cylindrical openings 32 leaving the conductive material elevationally below upper surfaces 47 of nitride rows 18 with an exemplary elevational difference being about 1,000 to about 1,500 angstroms. An exemplary conductive material includes undoped or doped polysilicon wherein the undoped polysilicon would be doped at some stage of the processing.

[0074] Still referring to Figs. 29-32, a conductivity implant (not shown) is performed to provide a conductivity dopant into upper surface portions 22 of substrate 12 to form diffusion regions or nodes 41. In one exemplary embodiment of the implant methods, the conductivity dopant is implanted substantially through posts 38 leaving substantially an entirety of the conductivity dopant within silicon substrate 12. Alternatively, a portion of the conductivity dopant remains in posts 38 to leave posts 38 electrically conductive forming a portion of the diffusion regions or nodes 41. Exemplary diffusion regions 41 comprise source/drain regions, for example, drain regions. In another exemplary

embodiment, posts 38 are conductively doped but do not form a portion of diffusion regions or nodes 41, and therefore, form electrical contacts between diffusion regions or nodes 41 of subsequently formed transistors and capacitors. In another still exemplary embodiment, posts 38 and diffusion regions 41 comprise an entirety of one of a pair of source/drain regions of a transistor with posts 38 electrically coupled to subsequently formed capacitors. In exemplary processing methods, a conductivity implant (not shown) is performed to provide a conductivity dopant substantially only into posts 38 and then posts 38 are annealed to out-diffuse conductivity dopant from posts 38 into silicon substrate 12 to form at least a portion of diffusion regions 41. In alternative exemplary embodiments, diffusion regions 41 are not formed wherein a conductivity implant (not shown) is performed to provide a conductivity dopant substantially only into posts 38 wherein posts 38 comprise an entirety of a one of a pair of source/drain regions. Alternatively, diffusion regions 41 comprise a portion of one of a pair of source/drain regions and posts 38 comprise another portion of the one of the pair of source/drain regions.

[0075] It should be understood that exemplary posts 38 are generally annular or cylindrical in shape and may or may not have empty space between optionally formed nitride liners 36 and/or TEOS spacers 34. A nitride material 40 is provided over substrate 12 and in cylindrical openings 32 to fill any empty space between posts 38, nitride liners 36 and/or TEOS spacers 34 and provide nitride material 40 over posts 38 and SOG layer 30. Nitride material 40 is etched back to form upper surfaces 49 that are recessed elevationally below the upper surfaces 37 of SOG layer 30 and below the upper surfaces 47 of nitride runners 18 (nitride material 40 is shown as having

incorporated optional nitride liners 36). Exemplary etches to recess nitride material 40 includes a planar or blanket reactive ion etch which recesses nitride material 40 to expose SOG layer 30 and TEOS spacers 34. An exemplary nitride material 40 is a sacrificial layer that serves as a barrier or hard mask 40 to protect epitaxial silicon posts 38 during subsequent processing, for example, removal of SOG layer 30 and TEOS spacers 34.

[0076] Referring to Figs. 33-36, a wet or vapor etch is performed to remove the SOG layer 30 and the TEOS spacers 34, and preferably to remove the SOG layer 30 and the TEOS spacers 34 entirely. An exemplary etch includes a selective etch to stop etching at nitride and silicon materials such as nitride liner 28, hard mask 40, nitride runners 18 and upper surface portions 22 of silicon substrate 12. The selective etch forms openings 42 defined by nitride liner 28, posts 38 (including hard mask 40), and nitride runners 18. Exemplary selective etches include a diluted hydrofluoric acid etch and/or a buffered oxide etch.

[0077] Referring to Figs. 37-40, a dry/wet nitride punch etch is performed to remove nitride liner 28 from over isolation regions 14, silicon substrate 12, and upper surface portions 22. The punch etch also removes portions of hard mask 40 from posts 38. In an exemplary embodiment, the thickness of hard mask 40 directly over posts 38 is substantially greater than the thickness of hard mask 40 over the sides of post 38 to allow the punch etch to remove side portions of hard mask 40 from posts 38 while leaving a substantial portion of hard mask 40 directly over posts 38.

[0078] Still referring to Figs. 37-40, a selective dry etch is performed to remove upper surface portions 22 of substrate 12 adjacent posts 38 and down to isolation

regions 14. The selective etch also removes portions of isolation regions 14 and leaves portions of silicon substrate 12 remaining directly below or beneath posts 38 and referred to as silicon support structures 46. Exemplary silicon support structures 46 are generally annular or cylindrical in shape, similar to posts 38 which extend elevationally above silicon support structures 46. The selective etch enlarges openings 42 to form openings 44 with a bottom periphery defined by silicon support structures 46, upper surface 48 of silicon substrate 12, and upper surface 50 of isolation regions 14. In one exemplary embodiment, the punch etch will etch or recess the silicon substrate 12 to slightly below the upper surface 50 of isolation regions 14 leaving upper surface 48 elevationally below upper surface 50.

[0079] Still referring to Figs. 37-40, an insulative film 52, for example an oxide, is formed over exposed portions of silicon substrate 12 and exposed portions of posts 38. The exposed portions of silicon substrate 12 include the bottom periphery of openings 44 defined by upper surfaces 48 and silicon support structures 46. The exposed portions of posts 38 include the sidewalls of posts 38. In one exemplary embodiment, insulative film 52 will comprise silicon dioxide and serve or function as a gate oxide or gate dielectric for subsequently formed transistors. An exemplary method of forming gate dielectrics 52 includes growing oxide on the exposed silicon surfaces of the upper surfaces 48, silicon support structures 46 and sidewalls of posts 38.

[0080] In one exemplary embodiment, silicon support structures 46 will serve or function as portions of channels for subsequently formed transistors. Accordingly, the length of silicon support structures 46, measured from the bottom portion of posts 38 to upper surface 48, will generally define a vertical length of a subsequently formed

transistor channel 46. Moreover, since the transistor channel 46 extends in a generally vertical or perpendicular orientation relative the orientation of substrate 12, and alternatively stated, since the transistor channel 46 extends perpendicularly to the horizontal or primary upper surface of substrate 12 (upper surface portions 22 not shown but existing as the interface between posts 38 and substrate 12), the transistor channel 46 will define an exemplary vertical transistor design in exemplary embodiments. Additionally, exemplary vertical transistor designs will include vertical surrounding transistors or vertical-surrounding-gate transistors in exemplary embodiments. It should be understood that the length of transistor channel 46 (alternatively referred to as vertical channel 46) will depend on the selective etch processing step, for example, the length of time the selective etch is allowed to remove and etch down into silicon substrate 12 (i.e., the depth of the selective etch into substrate 12).

[0081] Referring to Figs. 41-44, a conductive material is deposited over gate dielectrics 52 and will serve or function as transistor gates or word lines 54. An exemplary method of forming conductive material for transistor gates 54 includes depositing polysilicon material within openings 44, removing portions of the polysilicon material by CMP processing down to nitride runners 18, and then recessing the polysilicon material within openings 44 to below epitaxial silicon posts 38. For example, an upper surface 55 of transistor gates 54 is formed about 1,000 angstroms elevationally below upper surfaces 39 of epitaxial silicon posts 38. In one exemplary embodiment, polysilicon material of transistor gates 54 is recessed to form upper surfaces 55 elevationally below an upper surface of substrate 12 (for example, the

interface between posts 38 and substrate 12). An optional silicide layer (not shown) is formed over transistor gates 54 with exemplary silicides comprising titanium silicide and cobalt silicide.

[0082] Referring to Figs. 45-48, an insulative material or layer 56 is formed over silicon substrate 12, gate structures 54, epitaxial silicon posts 38 and nitride runners 18. Insulative layer 56 fills openings 44. Exemplary insulative layer 56 includes spin-on-glass layers and TEOS layers. Outermost portions of insulative layer 56 is removed by CMP or other planar etching methods to expose nitride runners 18 leaving insulative layer 56 extending in a line configuration between respective nitride runners 18. Next, nitride runners 18 are patterned and selectively etched to form openings 62 extending through portions of nitride runners 18 to expose upper surface portions 58 of substrate 12. It should be understood that portions of nitride runners 18 remain extending upward from and over silicon substrate 12. Exemplary upper surface portions 58 of silicon substrate 12 are configured generally as squares and bordered or surrounded by insulative layers 56 and the portions of nitride runners 18 that remain over silicon substrate 12. A conductivity implant (not shown) is performed to provide a conductivity dopant into upper surface portions 58 of substrate 12 to form active areas 59, for example, diffusion regions or nodes. In one exemplary embodiment, diffusion regions 59 will comprise source/drain regions 59 for subsequently formed devices, for example, transistors. In still another exemplary embodiment, diffusion regions 59 will comprise source/drain regions to complement and in operative cooperation with diffusion regions or nodes 41. Exemplary diffusion regions 59 comprise one of a pair of source/drain regions, for example, source regions.

[0083] Referring to Figs. 49-50, such illustrates a semiconductor construction 100 according to some exemplary embodiments at a processing stage subsequent to the processing stages of Figs. 1-48, for example, subsequent to the processing stages of Figs. 45-48. Fig. 49 represents a view orientation of semiconductor construction 100 similar to the view orientation of Fig. 46 at a subsequent processing stage. Fig. 50 represents a view orientation of semiconductor construction 100 similar to the view orientation of Fig. 48 at a subsequent processing stage. It should be understood that Fig. 50 is a view of the semiconductor construction 100 of Fig. 49 and rotated 90° from the orientation of the view for Fig. 49. Figs. 49-50 illustrate exemplary transistor devices electrically coupled with exemplary charge storage devices or data storage elements, for example, capacitor devices. Such exemplary combinations of transistors and capacitors are representative of memory and/or logic circuitry comprising memory cells such as DRAMs. An exemplary transistor device is referenced generally as numeral 69 and an exemplary charge storage device or data storage element, for example, a capacitor device is referenced generally as numeral 80.

[0084] An exemplary transistor 69 comprises a gate 54, a gate dielectric 52 and source/drain regions 41 and 59 (Fig. 50). Exemplary transistor 69 further includes a channel represented generally as the region of substrate 12 where current flow 71 is illustrated in Fig. 50 extending around gate 54 (and gate dielectric 52) from source/drain region 59 to source/drain region 41. An exemplary portion of the channel comprises silicon support structures 46 that extend directly elevationally below source/drain regions 41. Exemplary channel portions defined by silicon support structures 46 are cylindrical or annular portions of silicon substrate 12. Gate 54 extends generally

vertically downward into substrate 12 generally perpendicularly to an upper surface of silicon substrate 12 (upper surface represented generally as the horizontal top lines of source/drain regions 41 and 59, for example, the interface between posts 38 and source/drain regions 41). Gate 54 is spaced and insulated from silicon substrate 12 by gate dielectric 52. Gate 54 extends vertically relative silicon substrate 12. However, it should be understood that gate 54 surrounds or encircles the channel portion defined by silicon support structures 46. Accordingly, an exemplary gate 54 will define a vertical-surrounding-gate for a vertical transistor, for example, a vertical-surrounding-gate transistor. In an exemplary embodiment, if posts 38 are defined as electrical contacts and not as source/drain regions, an entirety of transistor 69 is formed within the silicon substrate or bulk wafer 12. Alternatively stated, transistor 69 is formed at or below an uppermost surface of wafer 12.

[0085] Exemplary source/drain regions 41 comprise drain regions. Exemplary source/drain regions 59 comprise source regions. In one exemplary embodiment, a single source/drain region 59 will comprise an entirety of the source region for transistor 69. In another exemplary embodiment, a pair of source/drain regions 59 formed on opposite sides of gate 54 will comprise an entirety of the source region for transistor 69. In one embodiment, activation of transistor 69 establishes current flow 71 from source region 59 downward through silicon substrate 12 below and around a bottom end of gate 54 and back upward through the channel portion 46 and to drain region 41. During processing subsequent to Figs. 45-48, hard masks 40 directly over posts 38 are removed and portions of insulative layer 56 directly over hard masks 40 are removed to expose upper surfaces of posts 38. Conductive material 102 is formed over and in

contact with posts 38 to form an electrical contact. Exemplary conductive material 102 is polysilicon to form polysilicon plugs or cell plugs 102 for electrical coupling transistors 69 via posts 38 to subsequently formed devices, for example, capacitors 80.

[0086] An exemplary capacitor 80 comprises a bottom cell plate or storage node 72, a capacitor dielectric 73 over storage node 72, and a top cell plate 74 over capacitor dielectric 73. Capacitor 80 is electrically coupled to transistor 69 by epitaxial silicon post 38 and polysilicon plug 102 with polysilicon plug 102 contacting and electrically coupled to storage node 72. Conductive plugs 61 (Fig. 50) are formed extending upward from and electrically coupled with source/drain regions 59. Conductive plugs 61 also contact portions of digit line 104 to electrically couple digit line 104 to transistors 69 via source/drain regions 59. Exemplary digit lines 104 comprise polysilicon and/or silicide layers. Exemplary conductive plugs 61 comprise doped polysilicon. Insulative spacers 70 (Fig. 50) are formed between conductive plugs 61 and insulative layer 56. Exemplary insulative spacers 70 comprise silicon nitride and/or oxide such as silicon dioxide.

[0087] Semiconductor construction 100 comprises intermediate structures between capacitors 80 and transistors 69. Nitride caps 106 are formed over digit line portions 104. Insulative spacers 110 are formed between digit lines 104 and nitride caps 106 on one side and polysilicon plugs 102 on the other side. A silicon dioxide layer 108 is formed over nitride caps 106.

[0088] In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and

described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

The invention claimed is:

1. A transistor device, comprising:
a semiconductor substrate; and
a gate extending within the semiconductor substrate, a gate dielectric over the gate, a pair of source/drain regions on opposite sides of the gate, and a channel region within the semiconductor substrate, at least a portion of the channel region defining the lowermost structure of the transistor device; and
wherein the gate encircles a portion of the semiconductor substrate.

2. The device of claim 1 wherein the gate dielectric, the pair of source/drain regions, and the channel region are within the semiconductor substrate.

3. The device of claim 1 wherein an entirety of gate dielectric, an entirety of the pair of source/drain regions and an entirety of the channel region are within the semiconductor substrate.

4. The device of claim 1 wherein the channel region is elevationally below the pair of source/drain regions within the semiconductor substrate.

5. The device of claim 1 wherein the semiconductor substrate comprises monocrystalline silicon.

6. The device of claim 1 further comprising the transistor incorporated into a DRAM device.

7. The device of claim 1 further comprising a data storage element electrically coupled to the transistor device to form a memory cell, the memory cell comprising an area of about $4F^2$ over the semiconductor substrate wherein F represents a minimum feature size for photolithographically-defined features.

8. The device of claim 1 wherein the portion of the semiconductor substrate comprises one of the pair of the source/drain regions.

9. The device of claim 1 further comprising a source/drain region in addition to the pair of the source/drain regions.

10. The device of claim 1 wherein a portion of one of the pair of source/drain regions comprises a pillar, and wherein an entirety of the gate is elevationally below an entirety of the pillar.

11. The device of claim 1 wherein a portion of one of the pair of source/drain regions comprises an epitaxial post, and wherein an entirety of the gate is elevationally below an entirety of the epitaxial post.

12. A transistor device, comprising:
a semiconductor substrate comprising an upper surface;
a pair of source/drain regions comprising portions of the semiconductor substrate; a channel region comprising at least three laterally-spaced portions within the semiconductor substrate and each of the three portions extending generally perpendicularly relative to the upper surface of the semiconductor substrate;
and a gate portion disposed between the pair of the source/drain regions, wherein one of the pair of the source/drain regions extends substantially vertically and defines the elevationally uppermost structure of the transistor device.

13. The device of claim 12 wherein one of the three portions of the channel region extends directly below the one of the pair of source/drain regions.

14. The device of claim 12 wherein one of the three portions of the channel region extends directly below the one of the pair of source/drain regions, and wherein the gate is within the semiconductor substrate and surrounds the one of the three portions of the channel region.

15. The device of claim 12 wherein the semiconductor substrate comprises monocrystalline silicon.

16. The device of claim 12 further comprising the transistor device incorporated into a DRAM device.

17. The device of claim 12 further comprising a data storage element electrically coupled to one of the pair of source/drain regions to form a memory cell, the memory cell comprising an area of about $4F^2$ over the semiconductor substrate wherein F represents a minimum feature size for photolithographically-defined features.

18. A semiconductor construction, comprising:
a conductive post extending upward from an upper surface of a semiconductor substrate, the conductive post comprising a circular cross section;
a source/drain region below the conductive post within the semiconductor substrate and electrically coupled with the conductive post;
a transistor channel extending below the source/drain region and comprising at least one curved portion of the semiconductor substrate; and
a gate within the semiconductor substrate adjacent the transistor channel, wherein the gate surrounds the source/drain region.

19. The construction of claim 18 wherein the conductive post comprises an epitaxial silicon post.

20. The construction of claim 18 wherein the source/drain region comprises a drain region.

21. The construction of claim 18 further comprising a capacitor electrically coupled with the conductive post.

22. The construction of claim 18 wherein the construction comprises a transistor, and further comprising incorporating the transistor into a memory cell structure wherein the conductive post electrically couples the transistor to a capacitor.

23. The construction of claim 18 wherein the semiconductor substrate is oriented generally horizontally and the transistor channel extends generally vertically.

24. The construction of claim 18 wherein the semiconductor substrate comprises monocrystalline silicon.

25. The construction of claim 18 further comprising:
another source/drain adjacent the gate opposite the transistor channel; and
a data storage element electrically coupled to the conductive post to form a memory cell, the memory cell comprising an area of about $4F^2$ over the semiconductor substrate wherein F represents a minimum feature size for photolithographically-defined features.

26. A vertical transistor structure, comprising: a silicon substrate;
a channel region defined within the silicon substrate and extending generally vertically relative the silicon substrate;
a first source/drain region elevationally above the channel region;
a gate laterally adjacent the channel region within the silicon substrate, at least a portion of the channel region being elevationally below an entirety of the gate;
a second source/drain region operatively proximate the gate;
a third source/drain region operatively proximate the gate; and wherein the gate surrounds another portion of the channel region.

27. The structure of claim 26 wherein the silicon substrate comprises monocrystalline silicon.

28. The structure of claim 26 wherein the first source/drain region comprises a drain region.

29. The structure of claim 26 wherein the gate surrounds the first source/drain region.

30. The structure of claim 26 wherein the first source/drain region is over the silicon substrate.

31. The structure of claim 26 wherein the first source/drain region is within the silicon substrate.

32. The structure of claim 26 wherein the silicon substrate comprises an upper surface, and wherein the first source/drain region comprises a portion extending from and elevationally below the upper surface and comprises another portion extending from and

elevationally above the upper surface.

33. The structure of claim 26 wherein the first source/drain region comprises an epitaxial post extending upward from the silicon substrate.

34. The structure of claim 26 wherein the first source/drain region comprises a diffusion region within the silicon substrate.

35. The structure of claim 26 wherein a portion of the first source/drain region comprises a diffusion region within the silicon substrate, and wherein another portion of the first source/drain region comprises an epitaxial post extending upward from the silicon substrate.

36. The structure of claim 26 further comprising an epitaxial post extending upward from the silicon substrate and electrically coupled to the first source/drain region, and wherein the epitaxial post comprises an electrical contact for the vertical transistor.

37. The structure of claim 26 further comprising an epitaxial post extending upward from the silicon substrate and directly over the first source/drain region, and wherein the epitaxial post comprises an electrical contact for the vertical transistor.

38. A transistor device, comprising:
a semiconductor substrate;
a gate extending within the semiconductor substrate, a gate dielectric over the gate, a pair of source/drain regions on opposite sides of the gate, and a channel region within the semiconductor substrate, at least a portion of the channel region defining the lowermost structure of the transistor device; and
wherein the gate surrounds another portion of the channel region.

39. The device of claim 38 wherein the gate surrounds one of the pair of the source/drain regions.

40. A vertical transistor structure, comprising: a silicon substrate;
a channel region defined within the silicon substrate and extending generally vertically relative the silicon substrate;

a first source/drain region elevationally above the channel region;
a gate laterally adjacent the channel region within the silicon substrate, at least a portion of the channel region being elevationally below an entirety of the gate;
a second source/drain region operatively proximate the gate;
a third source/drain region operatively proximate the gate; and wherein the gate surrounds the first source/drain region.

41. The structure of claim 40 wherein the gate surrounds another portion of the channel region.