

SEMICONDUCTOR PACKAGE ASSEMBLY AND MANUFACTURING METHOD

ABSTRACT

The embodiments of the disclosure provide a semiconductor package assembly and a manufacturing method. The semiconductor package assembly includes: a base plate having a first surface; a first chip structure located on the base plate and electrically connected to the first surface of the base plate; an intermediary layer having a first interconnection surface; and a molding compound. The first interconnection surface has a first interconnection region and a second interconnection region. A first solder ball is formed on the first interconnection region. A first pad is formed on the second interconnection region. The intermediary layer is electrically connected to the first surface of the base plate by means of the first pad. The molding compound seals the first chip structure, the intermediary layer and the first surface of the base plate. The first solder ball has a surface exposed from the molding compound. There is a preset height between the exposed surface of the first solder ball and the first interconnection surface of the intermediary layer.

[Fig. 1]