



Freely oscillating switched-mode power supply

The invention proceeds from a freely oscillating switched-mode power supply, in accordance with the preamble of Claim 1. Switched-mode power supplies having control only on the primary side of the isolating transformer have the advantage that there is no need of a transmission element for transmitting a controlled variable from the secondary side to the primary side of the isolated transformer, but the disadvantage that the voltages to be stabilised on the secondary side are not directly evaluated and thus the control for stabilising these voltages is frequently not sufficient. Switched-mode power supplies having control on the secondary side to the primary side have the advantage that effective stabilisation is achieved by the direct evaluation of the secondary-side voltages to be stabilised, but the disadvantage that an element such as, for example, an isolating transformer or an optocoupler is required to transmit a controlled variable from the secondary side to the primary side.

When such switched-mode power supplies in a television receiver are switched over for active standby operation to a low transmitted power of approximately 5-8 watts, the switching transistor would need to be switched on only for very short times. This can result in relatively high switching losses and risk to the switching transistor. It is therefore known in the case of operation with low transmitted power to switch on the switching transistor only in a packet-like or burst-like fashion with a sufficiently long turn-on time and sufficiently high current and to cause it to be blocked therebetween for a relatively long time during which absolutely no power is transmitted. Switched-mode power supplies which operate according to this principle are relatively complicated in design and generally require special integrated circuits.

The object of the invention is to provide a freely oscillating switched-mode power supply, which has pure primary control, can be realised by means of



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discrete subassemblies and requires no special ICs, renders possible automatic operation using PWM control for stabilisation in the case of full transmitted power and packet control in the case of low transmitted power, is short-circuit-proof, provides effective stabilisation despite the pure primary control, and has a good efficiency. This object is achieved by means of the invention specified in Claim 1. Advantageous developments of the invention are specified in the subclaims.

The switched-mode power supply according to the invention essentially has the following advantages: owing to control only on the primary side, there is no requirement for an element to transmit a controlled variable from the secondary side to the primary side such as, for example, an isolated transformer or an optocoupler. However, effective stabilisation of the operating voltages generated on the secondary side is achieved by PWM control in the case of normal operation at high power by controlled division of the cut-off voltage tapped from the shunt. Owing to the two circuits with different threshold values, there is an automatic transition from PWM control in normal operation to packet control in operation at low transmitted power. In this case, use is preferably made of subassemblies, already present, for switching on and realising these different modes of operation. The primary side forms an oscillator by means of which the switched-mode power supply is constructed in a freely oscillating fashion. Moreover, this oscillator has two functions. In the case of high transmitted power in normal operation, it effects continuous PWM control in driving the switching transistor, but on the other hand, in the case of low transmitted power, it automatically effects a pause in driving the switching transistor in order to achieve the described packet operation.

In a development of the invention in accordance with Claims 9 and 10, a negative internal resistance of the switched-mode power supply is simulated, which compensates the positive internal resistance inherently present, and thereby renders possible a switched-mode



power supply having a very low internal resistance. In another development of the invention in accordance with Claims 11-13, an additional circuit measure substantially improves the turn-off performance of the switching transistor at the start of the blocking phase. The invention can be advantageously applied, in particular, for relatively small television receivers, and likewise in the case of comparable units such as video recorders and CD players.

The invention is explained below with reference to three exemplary embodiments with the aid of the drawing, wherein

Figure 1 shows the complete circuit diagram of a switched-mode power supply according to the invention,

Figure 2 shows a simplified version of the circuit in accordance with Figure 1, and

Figure 3 shows a modification of the circuit according to Figure 2.

Figure 1 shows a freely oscillating switched-mode power supply having terminals 1 conducting the system voltage UN, the system bridge rectifier 2, the charging capacitor C1, the isolating transformer Tr, the switching transistor T1 and the shunt R1. The isolating transformer Tr contains the primary or power winding W1, the further primary winding W2, which constructs the circuit in a freely oscillating fashion and drives the switching transistor T1, and the regulating winding W3 which effects at the output b of the control rectifier 4 a control voltage Ur for stabilising and for switching over between operation at high power and low power. Tr contains, furthermore, a secondary winding W4 which generates a first operating voltage U2 at the terminals 6 via the rectifier 5, as well as a second secondary winding W5 which generates a further operating voltage U3 at the terminals 8 via the rectifier 7. Connected in the base line of the switching transistor T1 is a blocking voltage network, having the diodes D1, D2 and the capacitor C2, which generates a blocking voltage Uv.



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Furthermore, connected between the point a, which delivers the operating voltage U_1 for the switched-mode power supply, and the point c in the base line of the switching transistor T1 is the start circuit with the capacitor C3 and the resistor R2. The circuit as described so far is known.

The control voltage U_r passes from the point b to a first threshold circuit with the Zener diode Z1 and the transistors T2, T3. T3 is a component of a voltage divider R3, R4 which is connected between the point d and the base of the turn-off transistor T4, whose collector/emitter junction is connected in series with the diode D5 between the point c in the base line of the switching transistor T1 and earth.

Furthermore, U_r passes via the Zener diode Z1 and the voltage divider consisting of the resistors R5, R6 to the base of the transistor T5, whose collector is connected via the diodes D5, D9 to the base of the transistor T6. The collector thereof is connected to the base of the transistor T7, whose collector/emitter junction is connected in series with the resistor R7 in parallel with the coupling capacitor C4 in the base line of the switching transistor T1. The mode of operation of the circuit is explained separately below for normal operation at high power and operation at low power and packet control of T1.

In normal operation at high transmitted power of approximately 40-100 watts, U_r firstly becomes smaller due to the high load of the transformer Tr. U_r then passes via the conductive Zener diode Z1 to the base of T2, and via T3 switches in the resistor R4 more or less as a voltage divider resistor. The saw-tooth cut-off voltage U_s , which drops due to the saw-tooth current i_a in the flow phase from T1 to R1, now passes more or less divided to T4 and has the effect that at a specific value T4 becomes conductive, earths the point c, interrupts the base drive voltage for T1 and thereby turns off T1. Two limiting cases may now be considered. In the case of maximum load, that is to say minimum value of U_r , T2 is



blocked, as a result of which T3 becomes conductive. U_s is now divided in a maximum fashion by R3 and R4. This means that U_s must assume a larger final value at the point d in order to turn on T4. The current i_a thus reaches a high final value, and this corresponds to a large transmitted power. In the other limiting case, when the load at the terminals 6, 8 is low, U_r increases, so that now T2 becomes conductive and T3 is blocked. U_s is now not divided by R3 and R4 and passes at full value to the base of T4. This means that it is already the case at a low value of U_s and i_a that T4 becomes conductive and T1 is turned off. This means, in turn, a lower final value of i_a and thus a lower transmitted power. In normal operation between these limiting values, stabilisation of U_2 and U_3 is now performed by pulse-width modulation in the turn-on duration of T1. If, for example, the load at the terminals 6, 8 increases, the amplitude of all the pulse voltages generated at the transformer Tr drops, and thus also does that of the positive control voltage U_r . As a result, a less positive voltage U_r , reduced by the voltage of the Zener diode Z1, passes to the base of T2, so that T2 becomes less conductive and T3 more conductive. U_s is now divided more strongly by R3, R4, T3. This means that T4 does not become conductive until later and turns off T1, that is to say the final values of U_s and i_a assume larger final values, the transmitted power is increased and thus the reduction, assumed at the beginning, in the voltages U_2 , U_3 and U_r is compensated. T4 thus effects a pulse-width modulation in the driving of T1 to the effect that the turn-on duration of T1 is increased by T4 with increasing load. In this way, the operating voltages U_2 , U_3 that are generated are stabilised. Due to the voltage division by R5 and R6, T5 is still blocked in this case, as a result of which T6 and T7 are conductive. C4 is thereby bridged and has virtually no effect in this mode of operation.

If the load at the terminals 6, 8 is substantially reduced, for example in the case of active standby operation, the amplitude of the pulse voltages at the



transformer T_r , and thus the value of U_r , ~~increase~~. Despite the division by the voltage divider R_5 , R_6 , the transistor T_5 now becomes conductive and the point f more negative, as a result of which the transistors T_6 and thus also T_7 are blocked. The capacitor C_4 becomes effective in the base line of T_1 due to the blocking of T_7 . C_4 is thereby charged via the base/emitter diode of T_1 with the polarity represented, until finally the voltage at C_4 reaches the positive component of the voltage delivered by the winding W_2 and the switching transistor T_1 is blocked. The packet is thereby interrupted. There is then produced in the oscillation of T_1 a pause which effects the packet operation described at the beginning. T_1 now remains blocked for a certain time. As a result, the capacitors at the terminals 6, 8 are no longer recharged, so that U_r drops once again. At the end of the pause in the packet operation, T_5 is finally blocked once again, T_6 and T_7 become conductive once again, and the capacitor C_4 is bridged once again, so that the switching transistor T_1 is once again supplied with base current by the winding W_2 and oscillations are once again produced with full saturation of T_1 . Thus, the circuit represented effects automatic transition from normal operation at high transmitted power and PWM control in the driving of T_1 and the packet operation in which T_1 oscillates in each case only during the burst packets and does not oscillate therebetween for a time. In the packet operation, T_3 is always blocked, so that U_s passes undivided to the base of T_4 , and thus T_1 is already turned off in the case of a low current value of i_a .

The collector of T_5 , that is to say the point f , is still connected to the point c in the base line of T_1 . The following is achieved thereby. At the end of the pause during packet operation, T_5 is blocked once again, as described, so that a positive pulse which passes to the point c in the base line of T_1 occurs at the point f . It is achieved thereby that the first drive pulse once again effects full saturation of T_1 during the packet.



This has the advantage that turning on once again after the pause is not performed "softly" with a corresponding power loss and risk to T1, but to a certain extent in a "hard" fashion.

Further provided between the collector of T1 and point c is the circuit with the capacitor C5, the diode D6, the resistor R9, the diode D7, the resistor R10, the transistor T8 and the diode D8. This additional circuit serves to improve the blocking of the switching transistor T1 at the end of the turn-on phase, that is to say upon cutting of i_a , and operates as follows: the turn-on time of T1 is terminated inherently by the turned-on T4 by T4 cutting off the base current for T1. Thereafter, T1 remains conductive without base current for a certain time, owing to the saturation of charge carriers present in the transistor T1. T1 leaves saturation after a few μs without base current, as a result of which the collector becomes somewhat positive with respect to earth. This positive rise is transmitted to the base of T8 via the attenuation element with C5, D6 and R9, so that T8 becomes conductive and short-circuits the point c with respect to earth. In the meantime, the capacitor C2 is recharged with the represented polarity to the voltage U_v , specifically the sum of the forward voltages of D1 and D2. The conductive T8 thus earths the positive electrode of C2. As a result, the full voltage U_v becomes effective with negative polarity at the base of T1, so that turning off T1 is achieved in a conceivably short time. D7 serves to protect D8 against an excessively high negative voltage at the base. The overall result of the fact that T4 and T8 rapidly turn off T1 is a particularly small power loss in T1. The diode D8 between the collector of T8 and earth has the following task. Together with the diodes D1, D2, D3, D4 and R in the base line of T1, D8 stabilises the negative voltage fed by the winding W2 to the base of T1. The negative voltage delivered by the winding W2 is high in an inherently uncontrolled fashion, and can assume impermissibly high values at the base/emitter junction of



T1. The sub-assemblies D4, D3, D1, D2 and D8 serve to limit this negative voltage of, for example, greater than 5 volts at the base/emitter junction of T1. Moreover, an undesired inverse operation of T8 is thereby prevented. The negative voltages passing to the base of T1 are then both limited, specifically the negative voltage of C2 by the diodes D1 and D2, and the negative voltage from the winding W2 by the diodes D4, D3, D1, D2 and D8. An additional protection of T1 against an excessively high base/emitter voltage is achieved by means of this circuit.

The network C5, D6, R9 serves additionally as a so-called snubber for limiting positive voltage peaks at the collector of T1 at the start of the blocking phase of T1. The network thus advantageously has a double function, specifically improving the blocking of T1 at the start of the blocking phase and additionally limiting positive voltage peaks at the collector of T1. This is achieved when the inherently earthed right-hand end of the parallel circuit D6/R9 is not directly earthed but is connected to the base of the auxiliary switching transistor T8.

Provided further between the point d and the point b is the additional circuit 9 with the transistor T9, the capacitor C6 and the resistors R11, R12, R13. This circuit additionally serves to reduce the internal resistance at the outputs of the switched-mode power supply and operates in the following way in the manner of a controlled current sink: with increasing load, there is an increase in i_a and U_s at the point d due to the pulse-width control. As a result, T9 also becomes more conductive via the resistor R13. Owing to the filtering effect due to C6, an increased DC load which further reduces the value of U_r thus becomes effective at the point b. As a result, the control voltage path is simulated an additional reduction of U_r , and the effect of the reduced value of U_r is thus increased to increase the maximum value of U_s and i_a . The negative internal resistance formed by the circuit 9 is thus capable of

compensating the inherently still remaining positive internal resistance of the switched-mode power supply, and thus of ensuring for normal operation at high transmitted power a very low internal resistance of the switched-mode power supply.

Figure 2 shows a simplified version of the circuit according to Figure 1. The circuit according to Figure 2 does not contain the circuit 9 for forming a negative internal resistance, nor does it contain the transistor T7 which short-circuits the coupling capacitor C4 in the way described. Instead of the transistor T7, the coupling capacitor C4 is provided with a current path with the diode D10 and the resistor R15. In the case of packet operation, in this solution the base current for T1 varies in each case during a packet to the effect that the base current decreases towards the end of the packet. Since the circuit 9 for reducing the internal resistance is not present, it is possible to achieve a low internal resistance by improved coupling of the transformer Tr, for example by designing the transformer as a chamber winding transformer. The feature that the base current for T1 slightly decreases during a packet because the coupling capacitor C4 is not short-circuited can be tolerated in view of the simplification of the circuit. Moreover, a lower packet frequency of approximately 50 Hz can thereby be achieved. Such a low packet frequency in active standby operation is important, because it is inaudible, and therefore it is not possible for audible acoustic oscillations or vibrations of the unit to occur in active standby operation.

The capacitor C6 in parallel with the diode D11 in Figures 1 and 2 has a particular importance for the starting operation, that is to say in each case when the receiver is switched on, since then the diode D11 is firstly blocked. The capacitor C6 has a particular importance in the case of low system voltages, in order even then to ensure saturation of T1 and to avoid risk to T1 due to lack of saturation.

Figure 3 shows a modification of the circuit



according to Figure 2 which likewise operates without the circuit 9 of Figure 1 and without the transistor T7 for bridging the coupling capacitor C4. The mode of operation of the circuit in accordance with Figure 3 is similar to that of the circuit according to Figure 2.

In a circuit tested in practice, the sub-assemblies essential to the invention had the following values:

R1:	4.7 ohms	C2:	0.68 μF
R2:	22 kohms	C3:	4.7 μF
R3	220 ohms	C4:	47 μF
R4	22 ohms	C5:	470 pF
(start C)	(packet c)	(rectifier C)	
C3 :	C4	:	C (point b) = 1:10:100
4.7 μF	47 μF	:	470 μF
R5	100 kohms		
R6	100 kohms		
R7	10 ohms		
R9	220 ohms		
R10	470 ohms		
R11	100 ohms		
R12	10 ohms		
R13	100 ohms		
C6:	22 μF		

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Patent claims

1. Freely oscillating switched-mode power supply having a switching transistor (T1) and a transformer (Tr) with a power winding (W1), a drive winding (W2) delivering the switching voltage, and a regulating winding (W3) which delivers via a measuring rectifier (4) a control voltage (Ur) for varying the duration of current flow of the switching transistor (T1), a cut-off voltage (Us) tapped at the switching transistor (T1) by a shunt (R1) cutting off via a switch (T4) the base drive voltage at the switching transistor (T1), characterised in that the output (b) of the measuring rectifier (4) divides the cut-off voltage (Us) via a first circuit (Z1, T2, T3) with a first threshold value and switches on a coupling capacitor (C4) in the base line of the switching transistor (T1) via a second circuit (Z1, T5-T7) with a second threshold value.
2. Switched-mode power supply according to Claim 1, characterised in that the output (b) of the measuring rectifier (4) is applied via a Zener diode (Z1) to the control electrode of a transistor circuit (T2, T3) which forms a component of a first voltage divider (R3, R4) for the cut-off voltage (Us).
3. Circuit according to Claim 2, characterised in that the output of the first voltage divider (R3, R4) is connected to the base of a turn-off transistor (T4) whose collector/emitter junction is connected between the base line of the switching transistor (T1) and earth.
4. Circuit according to Claim 1, characterised in that the output (b) of the measuring rectifier (4) is connected via a threshold circuit to the control input of a transistor amplifier (T5-T7) whose output is connected in parallel with the coupling capacitor (C4) in the base line of the switching transistor (T1).
5. Circuit according to Claims 2 and 4, characterised in that a Zener diode (Z1) common to both circuits is connected, on the one hand, to the output (b) of the measuring rectifier (4) and, on the other hand, directly to the control input of the transistor circuit





(T2, T3) and via a voltage divider (R5, R6) to the control input of the switching amplifier (T5-T7).

6. Circuit according to Claim 5, characterised in that the output of the voltage divider (R5, R6) is connected to the base of a first transistor (T5) whose collector is connected to the base of a second transistor (T6) and whose collector is connected to the base of a third transistor (T7) whose collector/emitter junction is connected in parallel with the coupling capacitor (C4).

7. Circuit according to Claim 6, characterised in that the collector of the first transistor (T5) is additionally connected to a point (c) in the base line of the switching transistor (T1).

8. Circuit according to Claim 1, characterised in that there is connected between the regulating winding (W2) and the base of the switching transistor (T1) a diode circuit (D3, D4) polarised in such a way that when the switching transistor (T1) is turned off, an additional blocking voltage passes from the regulating winding (W2) to the switching transistor (T1).

9. Circuit according to Claim 1, characterised in that the peak value of the cut-off voltage (Us) is used to control a load (9) which is connected in parallel with the output (b) of the measuring rectifier (4).

10. Circuit according to Claim 9, characterised in that the cut-off voltage (Us) is applied to the base of a transistor (T9) whose collector is earthed via a capacitor (C6) and is connected via a resistor (R11) to the output (b) of the measuring rectifier (4), and whose emitter is earthed via a resistor (R12).

11. Circuit according to Claim 1, characterised in that the collector of the switching transistor (T1) is connected via an amplitude-selective circuit which responds to the positive pulse at the start of the blocking phase to the base of an auxiliary turn-off transistor (T8) whose collector/emitter junction is connected between a point (c) in the base line of the switching transistor (T1) and earth.

12. Circuit according to Claim 11, characterised in





that the collector of the auxiliary turn-off transistor (T8) is connected to the electrode, averted from the base of the switching transistor (T1), of a capacitor (C2) which is connected in the base line of the switching transistor (T1) and stores a blocking voltage (Us).

13. Circuit according to Claim 11, characterised in that the amplitude-selective circuit contains a snubber network composed of the series circuit of a capacitor (C5) and the parallel circuit of a resistor (R9) and a diode (D6).

14. Circuit according to Claim 11, characterised in that connected between the collector of the auxiliary turn-off transistor (T8) and earth is a diode (D8) which together with diodes (D1-D4) in the base line of the switching transistor (T1) limits the negative voltage at the base of the switching transistor (T1).

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