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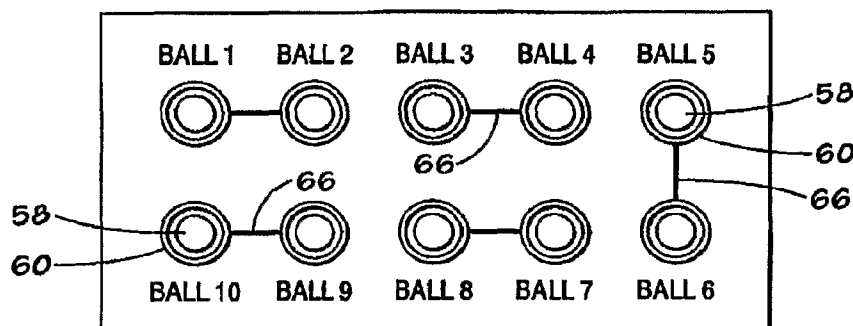
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(54) Title: CONNECTION VERIFICATION TECHNIQUE



(57) Abstract: Embodiments of the present invention are generally directed to testing connections of a memory device to a circuit board or other device. In one embodiment, a memory device that is configured to facilitate continuity testing between the device and a printed circuit board or other device is disclosed. The memory device includes a substrate and two connection pads (58) that are electrically coupled to one another via a test path (66). A system and method for testing the connections between a memory device and a circuit board or other device are also disclosed.