METHOD FOR PACKAGING AN OPTOELECTRONIC DEVICE AND PACKAGE FORMED THEREBY

Field of the Invention

The present invention relates in general to packaging an optoelectronic device, and more particularly to packaging an optoelectronic device at wafer level.

Background of the Invention

As is known, there are now packaged semiconductor optoelectronic devices that are used in such products as digital cameras, video cameras and the like. A packaged semiconductor optoelectronic device comprises a semiconductor optoelectronic integrated circuit or die, which is mounted on a substrate with electrical interconnections between pads on the optoelectronic semiconductor die, and leads on the substrate. The optoelectronic semiconductor die typically includes a photosensitive portion and a processor portion which, is coupled to the photosensitive portion. The processor portion receives signals from the photosensitive portion, and provides output signals at the leads of the package. These signals can then be used to produce an image on a display where the image is a result of light incident on the photosensitive portion.

The photosensitive portion is not glassivated and must not be contaminated with any foreign particles. The photosensitive portion comprises an array of picture elements or pixels. Each pixel can be only 25 microns ($25X10^{-6}$ meters) in diameter. Hence, any foreign particles that are at least the size of a pixel or larger, will adversely affect the performance of the optoelectronic device.

Typically, a glass or plastic window on the optoelectronic semiconductor package protects the photosensitive portion from contamination and damage, but allows incident light to fall thereon.

A conventional method of forming the packaged optoelectronic semiconductor device, starts by singulating the individual optoelectronic semiconductor die from a wafer, and mounting the semiconductor die with its back surface on the substrate and its front surface, with the photosensitive portion thereon, facing upwards away from the substrate. Using a wire bonding process short lengths of interconnecting wires are bonded between pads on the front surface and of the semiconductor die and lead portions on the substrate. The assembly of semiconductor die, substrate and interconnecting wires is then encapsulated with mold compound to form a packaged optoelectronic semiconductor device with an opening over the photosensitive portion. Typically, the opening is filled or covered by glass or plastic. This process is disclosed in US Patent No. 5897338 by Peter Jacobus Kaldenberg, and assigned to European Semiconductor Assembly (Eurasem) B.V. of the Netherlands.

Another method of packaging an optoelectronic semiconductor device is disclosed in PCT Patent Application No. PCT/US00/22836 by Glen et al. and assigned to Amkor Technology Inc. of USA. Here, the process is similar to the process disclosed by Kaldenberg above, except that the molding process uses an optically clear encapsulant, thus avoiding the need for forming the window during molding.

With known packaging processes, an optoelectronic semiconductor die is first singulated from a wafer, and a number of steps performed on the die before the die is encapsulated. Consequently, the die, and more importantly the photosensitive portion of the die, is left exposed from singulation through to encapsulation. To avoid contaminating the photosensitive portion of the die with foreign particles and adversely affecting the performance of the packaged optoelectronic semiconductor device, the processes from singulation

through to encapsulation is performed in a controlled environment. Such an environment is commonly referred to as a clean room, and for packaging optoelectronic semiconductor devices a Class 100 clean room is required. A Class 100 clean room is one wherein a contaminant level of 100 parts per million is maintained by special filtering and treatment of the air. Hence, a disadvantage of these packaging processes is the need for a Class 100 clean room, and the attendant high cost thereof.

European Patent Publication No. 1041628 by Beyne et al., assigned to Interununiversitair Microelektronica Centrum of Belgium, teaches covering each semiconductor optoelectronic die of a wafer, in particular the photosensitive portion of the die, with individual glass covers, and subsequently singulating the semiconductor dies. With the glass cover contamination of the photosensitive portion is avoided, and the glass covered optoelectronic die can be packaged without the need for a Class 100 clean room. The glass covers are made of material such as borosilicate, which tend to be expensive. Hence, a disadvantage of using the glass covers is the costs. Another disadvantage of using glass covers is the difficulty in handling the glass covers, as provisions must be made to prevent the glass covers themselves from becoming contaminated with foreign particles. Yet another disadvantage of Byne's process is the need to attach the 3.81-5.08 millimeter square glass covers with pick and place equipment in a Class 100 clean room.

Byne further teaches that the singulated glass covered optoelectronic die is then mounted on a substrate and interconnecting wires are bonded between pads on the optoelectronic die and leads on the substrate. The exposed pads, wire interconnects and portions of the leads are then encased in a sealant. Hence, another disadvantage of this process is the need for wire bonding, which has inherent handling problems when the wire interconnects are exposed, prior to application of the sealant. Another disadvantage of wire bonding is that it limits the height of the resultant package due to the internal clearance required within the package to accommodate the wire interconnects.

Brief Summary of the Invention

The present invention seeks to provide a method for packaging an optoelectronic device and package formed thereby which overcomes, or at least reduces, the abovementioned problems of the prior art.

Accordingly, in one aspect, the present invention provides a packaged optoelectronic device comprising:

a semiconductor die having a first surface with a photosensitive portion thereon; and

a transparent encapsulant disposed on and covering the photosensitive portion.

In another aspect the present invention provides a method for forming a packaged optoelectronic device, the method comprising the steps of:

a) disposing at least one layer of clear encapsulant on at least one photosensitive portion of an optoelectronic semiconductor die, the semiconductor die having pads thereon; and

b) flip chip mounting the semiconductor die on a substrate with the pads coupling to terminals on the substrate, the substrate having an opening therethrough with the photosensitive portion substantially aligned with the opening, and the substrate having external terminals coupled to the terminals.

In yet another aspect the present invention provides a method for encapsulating optoelectronic dies comprising the steps of:

a) providing a wafer comprising a plurality of optoelectronic dies, wherein each of the plurality of optoelectronic dies comprises at least one photosensitive portion thereon;

b) selectively forming a layer of clear encapsulant on each of the photosensitive portions on the wafer; and

c) singulating the semiconductor dies from the wafer.

Brief Description of the Drawings

An embodiment of the present invention will now be more fully described, by way of example, with reference to the drawings of which:

FIG. 1 shows a side sectional view of a semiconductor optoelectronic package in accordance with the present invention;

FIG. 2 shows a flow chart detailing the process for forming the package in FIG. 1;

FIG. 3 shows an enlarged view of a portion of a semiconductor wafer when forming a layer of clear encapsulant thereon for packaging in the semiconductor optoelectronic package in FIG. 1;

FIG. 4 shows a flow chart detailing a process for forming the layer of clear encapsulant in FIG. 3;

FIG. 5 shows a side sectional view of a semiconductor optoelectronic package in accordance with an alternate embodiment of the present invention; and

FIG. 6 shows a flow chart detailing the process for forming the package in FIG. 5.

Detail Description of the Drawings

A layer of clear encapsulant is disposed and cured on the photosensitive portions of optoelectronic dies of a semiconductor wafer, to provide a protective cover over the photosensitive portions of the dies. While the steps of disposing and curing the encapsulant, must necessarily be carried out in a Class 100 clean room, subsequent packaging steps can now, advantageously be performed without the need for a Class 100 clean room. In addition, the semiconductor optoelectronic die with the layer of encapsulant can be flip chip mounted onto a substrate to form a flip chip semiconductor optoelectronic package, without the need for Class 100 clean room. Alternatively, the semiconductor die with the encapsulant can be wire

bonded to leads on a substrate to form a wire bonded semiconductor optoelectronic package, again, without the need for Class 100 clean room.

FIG. 1 shows a semiconductor optoelectronic package 100 with a semiconductor die 105 having a photosensitive portion 110 thereon. A layer 115 of clear epoxy encapsulates the photosensitive portion 110. An example of the clear epoxy is HL880 manufactured by Dexter Ltd. of Japan. The layer 115 of clear epoxy has a thickness of 0.254 to 0.381 millimeters. Pads 120 on the die 105 have bumped interconnects 125 thereon, and the bumped interconnects 125 adhere to terminals 130 on a substrate 135. The bumped interconnects 125 can comprise solder, polymer bumps or nickel/gold eutectic, and can also include pillar bumps such as those made of copper. The substrate 135 has an opening 137 therethrough, and when the die 105 is mounted to the substrate 135 by the bumped interconnects 125, the photosensitive portion 110 is aligned with the opening 137. The opening 137 allows incident light access to the photosensitive portion 110.

The substrate 135 in turn has solder balls 145 mounted on external terminals 140 to provide external connections for the package 100. Typically, the solder balls 145 are eutectic solder balls. The package 100 can further include a lens holder 150 mounted on the substrate 135 by epoxy 152, and the lens holder 150 holds a lens 155 over the opening 137.

In FIG. 2 a process 200 for forming the package 100 starts 205 with the step of disposing 210 the layer 115 of clear epoxy encapsulant on the photosensitive portions 110 of the optoelectronic dies of a semiconductor wafer in a Class 100 clean room. The semiconductor wafer with the layer 115 of clear epoxy encapsulant is then heated at a temperature of 100 degrees Celsius for 2 hours, and then at 125 degrees Celsius for an additional 4 hours in an oven, such as a force convection oven manufactured by Blue-M of the USA, to cure 215 the layer 115 of clear epoxy encapsulant. Upon curing, the layer 115 of

clear epoxy encapsulant forms a protective cover over the photosensitive portion 110. With the protective cover, the semiconductor wafer can be further processed with a reduced risk of adversely affecting the photosensitive portion 110 by contamination or damage.

Next, when the semiconductor wafer is to be bumped, the bumping 220 process is also performed in a Class 100 clean room. An example of such a bumping process is described in US patent application Serial No. 09/564,382 by Francisca Tung, filed on April 27, 2000, titled "Improved Pillar Connections For Semiconductor Chip", and Continuation-In-Part US patent application Serial No. 09/843,248 by Francisca Tung, filed on April 27, 2001 titled "Pillar Connections For Semiconductor Chips and Method Of Manufacture", and assigned to a common assignee as this patent application, teaches forming pillar bumped structures as described herein. These patent applications are incorporated herein by reference thereto. Alternatively, other bumping processes that form solder bumps using eutectic or high lead solder can also be employed.

Typically, the semiconductor wafer is produced at a wafer fabrication facility and transported to a wafer bumping service provider's facility for bumping. In accordance with the present invention, the wafer bumping service provider can advantageously dispose the layer 115 of clear epoxy encapsulant on the photosensitive portion 110 of the semiconductor wafer, and then proceed with the bumping process. Hence, after applying the layer of clear epoxy encapsulant and bumping a semiconductor wafer, the semiconductor wafer can then be conveniently transported and further subjected to packaging processes in a typical semiconductor packaging environment, such as a Class 5,000-10,000 clean room.

Packaging continues with singulating 225 the die 105 from the semiconductor wafer, and mounting the die 105 on the substrate 135. During mounting the pattern of bumps 125 is aligned with a corresponding pattern of pads 120 on the substrate 135, and

subsequently, the die 105 is placed on the substrate 135 with the pattern of bumps 125 abutting the pattern of pads 120. The assembly of die 105 and substrate 135 is then reflowed 235.

During reflow, the pads 120, typically eutectic solder paste, melts and form interconnects, thus electrically coupling the pads 120 on the die 105 to the terminals 130 on the substrate 135. Solder balls 145 are then disposed 240 on the external terminals 140, and the assembly with the solder balls 145 is reflowed 245 for the solder balls 145 to melt and adhere to the external terminals 140, ending 250 the process 200.

The process 200 can include additional steps for mounting the lens holder 150 on the substrate 135 with adhesive, where the lens holder 150 holds the lens 155 over the opening 137 in the substrate 135. The process 200 can further include a step of disposing encapsulant on the back of the die 105 to prevent damage to the die 105 when the package 100 is mounted on a printed circuit board, for example.

With reference to FIGS. 3 and 4, a process 400 of forming a layer of clear epoxy encapsulant over the photosensitive portions 315 of dies 310 of a semiconductor wafer 305 starts 405 with aligning a stencil 330 with the semiconductor wafer 305 and disposing the stencil 330 on the semiconductor wafer 305. The stencil 330 comprises a metal sheet patterned with openings 335 that delineate areas around the photosensitive portions 315 that are to be filled with the clear epoxy encapsulant. The side of the stencil 330 that abuts the upper surface of the semiconductor wafer 305 is coated with a layer of Teflon® to prevent the stencil 330 from sticking to the semiconductor wafer 305. Alternatively, the stencil may be made of non-metallic material such as any high temperature rubber.

The stencil 330 must have a predetermined thickness of 10-15 mils in order to form a layer of the clear epoxy encapsulant having the required thickness. Typically, the clear epoxy encapsulant should have a thickness of 5-10 mils. It is important that the thickness of the clear epoxy encapsulant is equally distributed, so as not to adversely affect

the solder ball stand-off during mounting of the semiconductor optoelectronic package 100.

Next, the clear epoxy encapsulant is applied 430 over the upper surface of the stencil 330. This can be accomplished using screen-printing or extrusion coating. Then with the stencil 330 still in place on the semiconductor wafer 305, the semiconductor wafer 305 and the stencil 330 is placed in an oven and the clear epoxy encapsulant is cured at a temperature of 100 to 125 degrees Celsius for a period of 3 to 4 hours. Again, the force convection oven manufactured by Blue-M may be used.

The clear encapsulant has a low viscosity and the stencil 330 is held in place on the semiconductor wafer 305 during dispensing 430 and curing 435 to prevent the clear epoxy encapsulant from flowing away from the photosensitive portions 315. After curing, the stencil is removed 440 and the clear epoxy encapsulant forms the layer 115 on the photosensitive portions 315 that protects the photosensitive portions 315 from contamination and damage, and does not substantially affect the performance of the optoelectronic die 105. The process 400 then ends 445.

FIG. 5 shows a wire-bonded semiconductor optoelectronic package 500 with the semiconductor die 105 having the photosensitive portion 110 thereon. As described earlier, a layer 115 of clear epoxy encapsulates the photosensitive portion 110. Here, the semiconductor die 105 has pads 505 suitable for wire bonding. The semiconductor die 105 is mounted on a substrate 502, typically with epoxy, and wire interconnects 510 are coupled to the pads 505 and terminals 515 on the substrate. Typically, gold wire is used in conjunction with a wire bonding process as is known in the art.

The terminals 515 are coupled to external terminals 525 on an opposite surface of the substrate 502, and solder balls are attached to the external terminals 525.

With reference to FIG. 6 a process 600 for forming the package 500 starts 602 with the step of disposing 604 the layer 115 of clear epoxy encapsulant on the photosensitive portions 110 of the optoelectronic dies of a semiconductor wafer in a Class 100 clean room. The semiconductor wafer with the layer 115 of clear epoxy encapsulant is then heated at a temperature in an oven, as before, to cure 606 the layer 115 of clear epoxy encapsulant. With the protective cover, the semiconductor wafer can be further processed with a reduced risk of adversely affecting the photosensitive portion 110 by contamination or damage.

Typically, after the semiconductor wafer is produced at a wafer fabrication facility, the wafer is transported to a packaging facility, which typically has a Class 5,000-10,000 clean room. At the packaging facility, when the constituent dies of the semiconductor wafer are to be wire bonded, the wafer is singulated 608.

Next, each of the semiconductor dies 105 is mounted 610, typically with epoxy, on a substrate 502, and wire interconnects 510 are bonded 612 to connect each pad 505 on the semiconductor die 105 to a terminal 515 on the substrate 502. The wire bonding process is known to one skilled in the art, and will not be described further herein. Next, the semiconductor die 105 and the wire interconnects 510 are encapsulated 614 in clear epoxy 520, ending 616 the process 600. The substrate 502 includes traces therein that connect to external terminals 525, and solder balls 530 can be attached to the external terminals 525 to facilitate mounting the semiconductor package 500.

Hence, the present invention, as described can be employed in wire bonded semiconductor optoelectronic packages as well as flip chip semiconductor optoelectronic packages.

The present invention, as described, provides an optoelectronic semiconductor package where a photosensitive portion of an optoelectronic die is encapsulated with a layer of clear epoxy when the die is part of a wafer. This advantageously allows the optoelectronic die

to be subsequently handled and packaged in a typical semiconductor packaging facility, without the need for a Class 100 clean room.

The present invention therefore provides a method for packaging an optoelectronic device and a package formed thereby which overcomes, or at least reduces, the abovementioned problems of the prior art.

It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.

CLAIMS

1. A packaged optoelectronic device comprising:

a semiconductor die having a first surface with a photosensitive portion thereon; and

a transparent encapsulant disposed on and covering the photosensitive portion.

2. A packaged optoelectronic device in accordance with claim 1 further comprising a substrate having an opening therethrough, wherein the semiconductor die is mounted on the substrate, the first surface of the semiconductor die adjacent a first surface of the substrate, with the photosensitive portion substantially aligned with the opening in the substrate.

3. A packaged optoelectronic device in accordance with claim 2 wherein the semiconductor die further comprises pads on the first surface and wherein the first surface of the substrate comprises corresponding terminals thereon, and wherein interconnects couple the semiconductor pads to the corresponding terminals.

4. A packaged optoelectronic device in accordance with claim 3 wherein at least a portion of each interconnect comprises reflowable material.

5. A packaged optoelectronic device in accordance with claim 3 wherein at least a portion of each interconnect comprises non-reflowable material.

6. A packaged optoelectronic device in accordance with claim 3 wherein at least a portion of each interconnect comprises solder, and at least another portion of the each interconnect comprises solid metal.

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7. A packaged optoelectronic device in accordance with claim 3 wherein the substrate further comprises external terminals coupled to the terminals by a predetermined pattern of traces therein.

8. A packaged optoelectronic device in accordance with claim 7 wherein the external terminals are on the first surface of the substrate.

9. A packaged optoelectronic device in accordance with claim 7 wherein the substrate comprises a second surface opposite the first surface thereof, and wherein the external terminals are on the second surface of the substrate.

10. A packaged optoelectronic device in accordance with claim 7 wherein conductive deposits are disposed on the external terminals.

11. A packaged optoelectronic device in accordance with claim 10 wherein at least a portion of each conductive deposit comprises reflowable material.

12. A packaged optoelectronic device in accordance with claim 10 wherein at least a portion of each interconnect comprises non-reflowable material.

13. A packaged optoelectronic device in accordance with claim 10 wherein at least a portion of each conductive deposit comprises reflowable material, and at least another portion of the each conductive deposit comprises non-reflowable material.

14. A packaged optoelectronic device in accordance with claim 10 further comprising a lens mounted on the substrate, wherein the lens is aligned with the opening.

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15. A packaged optoelectronic device in accordance with claim 14 further comprising a lens holder adapted to receive the lens, and the lens holder for mounting the lens on the substrate.

16. A method for forming a packaged optoelectronic device, the method comprising the steps of:

a) disposing at least one layer of clear encapsulant on at least one photosensitive portion of an optoelectronic semiconductor die, the semiconductor die having pads thereon; and

b) flip chip mounting the semiconductor die on a substrate with the pads coupling to terminals on the substrate, the substrate having an opening therethrough with the photosensitive portion substantially aligned with the opening, and the substrate having external terminals coupled to the terminals.

17. A method in accordance with claim 16 wherein step (a) comprises the steps of:

a1) providing a wafer comprising a plurality of optoelectronic dies, wherein each of the plurality of optoelectronic dies comprises at least one photosensitive portion thereon;

a2) selectively forming clear encapsulant on each of the photosensitive portions on the wafer; and

a3) singulating the semiconductor dies from the wafer.

18. A method in accordance with claim 17 wherein step (a2) comprises the steps of:

disposing a stencil on the wafer;

dispensing clear encapsulant on each of the photosensitive portions;

curing the clear encapsulant; and

removing the stencil from the wafer.

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19. A method in accordance with claim 18 wherein the step of dispensing the clear encapsulant on each of the photosensitive portions comprises the step of extrusion coating.

20. A method in accordance with claim 18 wherein the step of dispensing the clear encapsulant on each of the photosensitive portions comprises the step of screen printing.

21. A method in accordance with claim 16 wherein step (b) comprises the steps of:

b1) bumping the pads on the semiconductor die;

b2) disposing reflowable material on the terminals of the substrate;

b3) placing the semiconductor die on the substrate with the bumps abutting the reflowable material; and

b4) reflowing the semiconductor die and the substrate to form the reflowable material into interconnects.

22. A method in accordance with claim 21 wherein step (b1) comprises the step of disposing deposits of non-flowable material on the pads.

23. A method in accordance with claim 21 wherein step (b1) comprises the step of disposing deposits of non-flowable material on the pads, and subsequently disposing a layer of reflowable material on the deposits of non-flowable material.

24. A method for encapsulating optoelectronic dies, comprising the steps of :

a) providing a wafer comprising a plurality of optoelectronic dies, wherein each of the plurality of optoelectronic dies comprises at least one photosensitive portion thereon;

b) selectively forming a layer of clear encapsulant on each of the photosensitive portions on the wafer; and

c) singulating the semiconductor dies from the wafer.

25. A method in accordance with claim 24 wherein step (b) comprises the steps of:

disposing a stencil on the wafer;

dispensing a layer of clear encapsulant on the photosensitive portions;

curing the clear encapsulant; and

removing the stencil from the wafer.

26. A method in accordance with claim 25 wherein the step of dispensing comprises the step of extrusion coating.

27. A method in accordance with claim 25 wherein the step of dispensing comprises the step of screen printing.