METHOD FOR ESTABLISHING ULTRA-THIN GATE INSULATOR USING ANNEAL IN AMMONIA

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This application claims the benefit of U.S. Provisional Application No. 60/169,540, filed on December 7, 1999 and entitled "METHOD FOR ESTABLISHING ULTRA-THIN GATE INSULATOR USING ANNEAL IN AMMONIA".

TECHNICAL FIELD

The present invention relates to the fabrication of semiconductor devices, and more particularly to establishing field effect transistor (FET) gate insulators.

BACKGROUND ART

Semiconductor chips or wafers are used in many applications, including as integrated circuits and as flash memory for hand held computing devices, wireless telephones, and digital cameras. Regardless of the application, it is desirable that a semiconductor chip hold as many circuits or memory cells as possible per unit area. In this way, the size, weight, and energy consumption of devices that use semiconductor chips advantageously is minimized, while nevertheless improving the memory capacity and computing power of the devices.

It can readily be appreciated that it is important to electrically isolate various components of an integrated circuit from each other, to ensure proper circuit operation. As one example, in a transistor, a gate is formed on a semiconductor substrate, with the gate being insulated from the substrate by a very thin dielectric layer, referred to as the "gate oxide" or "gate insulator". As the scale of semiconductor devices decreases, the thickness of the gate insulator layer likewise decreases.

As recognized herein, at very small scales, the gate insulator can be become so thin that otherwise relatively small encroachments into the gate insulator layer by sub-oxides from the substrate and from adjacent polysilicon connector electrodes can reduce the insulating ability of the gate insulator layer. This poses severe problems because under these circumstances, even very minor defects in the substrate can create electron leakage paths through the gate insulator, leading to catastrophic failure of the transistor.

To circumvent this problem, alternatives to traditional gate oxide materials, such as high-k dielectric materials including nitrides and oxynitrides that can be made very thin and still retain good insulating properties, have been proposed. Unfortunately, it is thought that these materials can degrade the performance of the transistor. Nitride, in particular, has been considered undesirable because it promotes unwanted leakage of electrons through the gate insulator layer.

Furthermore, as the gate insulator layer becomes very thin, e.g., on the order of nineteen Angstroms (19A), device integration becomes highly complicated. Specifically, it is necessary to etch portions of the polysilicon electrodes down to the substrate, but stopping the etch on a very thin, e.g., 19A gate insulator layer without pitting the substrate underneath becomes problematic. Accordingly, the present invention recognizes that it is desirable to provide a gate insulator layer that can be made very thin as appropriate for very small-scale transistors while retaining sufficient electrical insulation properties to adequately function

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as a gate insulator, and while retaining sufficient physical thickness to facilitate device integration, without degrading performance vis-a-vis oxide insulators.

EP-A-0,847,079; US-A-4,490,900; US-A-5,254,489; US-A-5,219,773; US-A-5,656,516; US-A-5,017,979; and the article by Naito et al entitled 'Effect of Nitrogen Distribution in Nitrided Oxide Prepared by Rapid Thermal Annealing on its Electrical Characteristics', (Journal of Vacuum Science and Technology: Part B, vol.5, no.3, May 1987, pages 633-637) disclose various methods for making a semiconductor device in which an oxide film is established on a semiconductor substrate and the substrate is then subjected to further processing before forming FET gates on portions of the film.

According to one aspect of the present invention there is provided a method for making a semiconductor device, having an ultra-thin insulator for inhibiting tunneling effects, said method comprising: providing a semiconductor substrate; establishing an oxide base film on the substrate, said oxide base film having a, wherein said step of establishing the oxide base film comprises said oxide film thickness of no more than twenty-four Angstoms (≤ 24 Å); characterised by annealing the oxide base film on the substrate in an ammonia (NH_3) environment in a temperature range of up to eleven hundred degrees Celsius (1100°C), thereby forming a nitrided oxide film, wherein the step of annealing reduces the effective electrical thickness of the nitrided oxide film to twenty Angstroms (20 Å), the nitrided oxide film thickness relative to said oxide base film thickness facilitating inhibition of said tunneling effects, thereby resulting in a lower standby current for a higher drive current and capacitance, for facilitating function as a gate insulator, and for facilitating integration of said device, said nitrided oxide film having electrical insulating properties equal to that of an oxide film thinner than said oxide base film thickness, and said ultra-thin insulator comprising said nitrided oxide film; and forming at least one polysilicon-based field effect transistor (FET) gate on at least one portion of the nitrided oxide film.

For a better understanding of the invention, reference is made to the accompanying drawings wherein, by way of example only:

Figure 1 is a flow chart of a process for manufacturing a semiconductor device;

Figure 2 is a side view of the device after forming the base film on the substrate;

Figure 3 is a side view of the device after annealing the base film; and

Figure 4 is a side view of the device after forming the FET gate stacks on the nitride film.

The principles of the present invention are equally applicable to a wide range of semiconductor and integrated circuit design and manufacture regimens, including but not necessarily limited to the production of non-volatile memory devices. All such implementations are specifically contemplated by the principles of the present invention.

Referring initially to Figures 1 and 2, at block 10 in Figure 1 a semiconductor substrate 12 (Figure 2) such as Silicon is provided, and then at block 14 a thin Oxide base film 16 is grown on the substrate 12 in accordance with oxide film formation principles known in the art, in direct contact with the substrate 12. The thickness "t" of the base film 16 is no more than twenty four Angstroms (24Å).

Moving to block 18 of Figure 1 and referring to Figure 3, the substrate 12 with film 16 is annealed in situ in ammonia (NH_3) at a temperature of up to eleven hundred degrees Celsius (1100°C) to establish a Nitrogen concentration in the base film 16, thereby forming the nitrided oxide film. The Nitrogen is represented by the dots 19. In accordance with present principles, after annealing, the electrically insulating properties of the nitrided oxide film corresponds to that of a conventional oxide film having a physical thickness of only 20A, (yet having a physical thickness nearly equal to the film 16 prior to annealing) to inhibit undesired

tunnelling through the nitrided oxide film, thereby resulting in a relatively lower standby current for a relatively higher drive current and capacitance.

Next, at block 20 in Figure 2 and referring now to Figure 4, a polysilicon -based field effect transistor (FET) stack 28 is formed on the film 16 in accordance with FET gate stack deposition and patterning principles known in the art. After forming and patterning the FET stacks 28, the process is completed by forming FET sources and drains 36, 38 using conventional principles, and contacts, interconnects, and FET to FET insulation are likewise conventionally undertaken.

With the above disclosure in mind, the ammonia anneal of the base film reduces the equivalent electrical thickness of the base film. In other words, for a film that is sufficiently thick for the abovementioned structural considerations, e.g., 24A thick, after annealing the film advantageously behaves electrically like a film that is only 20A thick. This in turn advantageously decreases subsequent electron tunneling resulting in a lower standby current for higher drive current and capacitance, compared to a film not annealed in ammonia.

In the present description, and in the accompanying claims, the term "electrical thickness" is defined as "having the same electrical resistance as the same film of reduced thickness".

CLAIMS:

1. A method for making a semiconductor device, having an ultra-thin insulator for inhibiting tunneling effects, said method comprising:

providing a semiconductor substrate (12);

establishing an oxide base film (16) on the substrate, said oxide base film having a thickness of no more than twenty-four Angstoms ($\leq$ 24 Å); characterised by

annealing the oxide base film (16) on the substrate (12) in an ammonia (NH_3) environment in a temperature range of up to eleven hundred degrees Celsius (1100°C), thereby forming a nitrided oxide film,

wherein the step of annealing reduces the effective electrical thickness of the nitrided oxide film to twenty Angstroms (20 Å),

the nitrided oxide film thickness relative to said oxide base film thickness facilitating inhibition of said tunneling effects, thereby resulting in a lower standby current for a higher drive current and capacitance, for facilitating function as a gate insulator, and for facilitating integration of said device,

said nitrided oxide film having electrical insulating properties equal to that of an oxide film thinner than said oxide base film thickness, and

said ultra-thin insulator comprising said nitrided oxide film; and

forming at least one polysilicon-based field effect transistor (FET) gate (28) on at least one portion of the nitrided oxide film.

2. A method, as claimed in Claim 1, wherein the step of annealing decreases subsequent electron tunneling through the nitride oxide film, thereby resulting in a lower standby current for higher drive current and capacitance than the oxide base film would have.