HATTED POLYSILICON GATE STRUCTURE FOR IMPROVING SALICIDE PERFORMANCE AND METHOD OF FORMING THE SAME

ABSTRACT

Alternate methods of forming low resistance "hatted" polysilicon gate elements are provided that increase the effective area in the polysilicon gate for silicide grain growth during silicide formation. The expanded top portion helps to prevent silicide agglomeration in the silicide regions, thereby maintaining or reducing electrode resistance, improving high-frequency performance, and reducing gate delay in sub micron FET ULSI devices, without increasing the underlying active channel length.